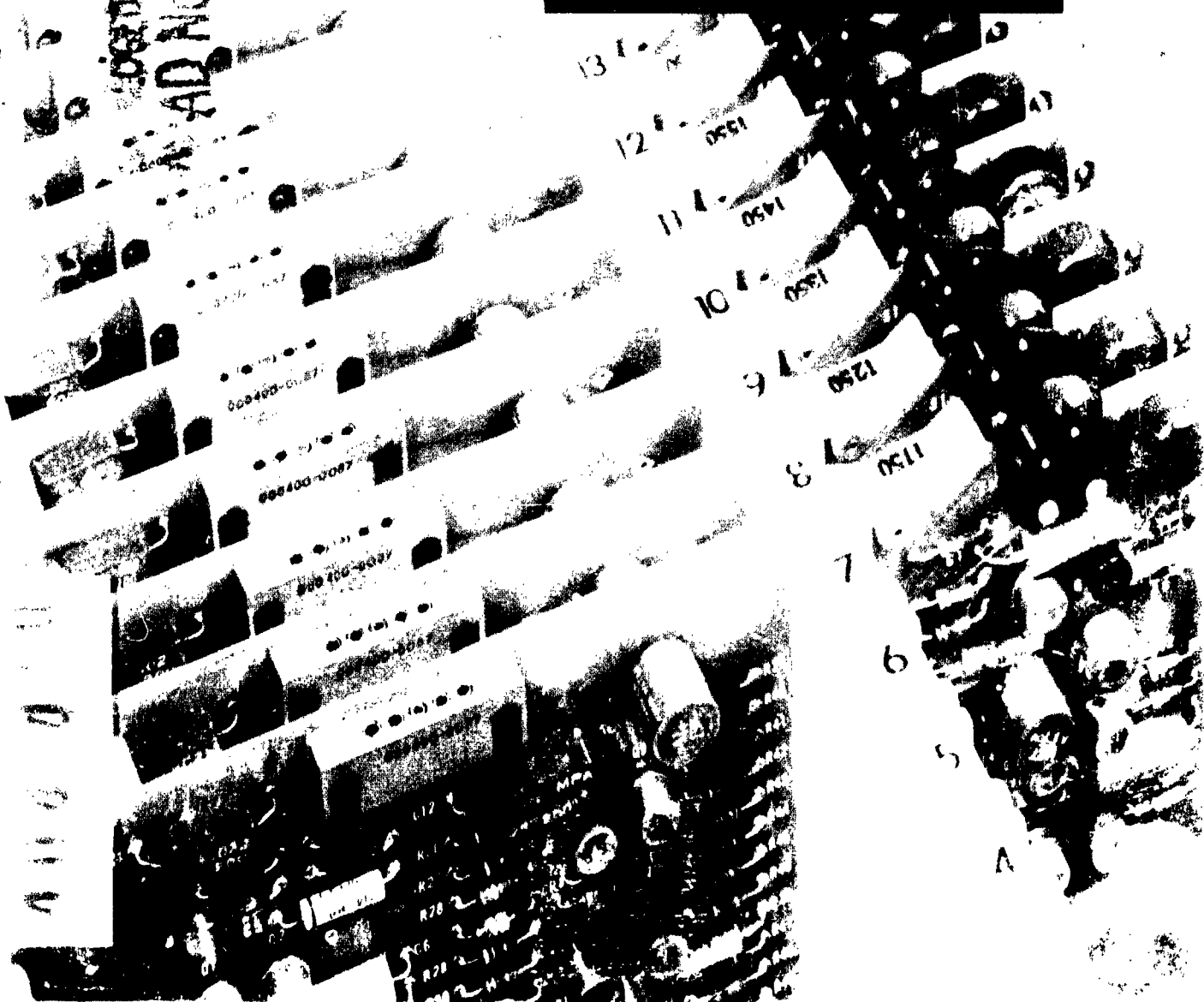SANTA ANA FREEWAY AT EUCLID AVE. ANAHEIM, CALIFORNIA

AERONAUTICAL & INSTRUMENT DIVISION
ROBERTSHAW-FULTON CONTROLS COMPANY

909-026-019

FINAL ENGINEERING REPORT

"MULTILOK"* HIGH SPEED DATA MODEM

MODEL 6005

This report has been approved for general distribution.

MARCH 1, 1963

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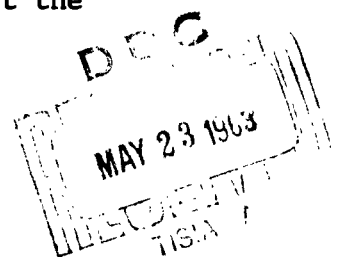official views or policy of the FAA.

MAY 23 1963

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*Trademark

ABSTRACT

The Robertshaw Multilock* high speed data modem was
adapted for operation with a ground-air-ground digital
communications link. The modems employ phase-shift
modulation techniques with synchronized data rates up to
1200 bits per second. Solid state components are used
throughout the equipment.

Error rates of less than 1 in 10^5 bits were recorded
for line signal-to-noise ratios of 15 db or greater.
Error free data transmission was achieved in the absence
of noise over a dynamic range of 50 db on the demodulation
input.

*Pats. Pending

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SECTION I

DESCRIPTION

1.1 GENERAL.

The Multilok High Speed Data Modem Model 6005 (figure 1-1) manufactured by Robertshaw-Fulton Controls Company, Aeronautical and Instrument Division, Anaheim, California, was designed for use in single-channel simplex (scs) ground and airborne systems. It provides a two-way data communication link between ground stations and aircraft for handling essential flight data by means other than verbal communication (figure 1-2).

The modem is assembled on a single chassis which contains modulator and demodulator band pass filters, a low pass filter, and modulator and demodulator circuit boards (figure 1-3). All active elements are solid state mounted on glass-epoxy etched circuit boards. Figure 1-4 is a block diagram of the subsystem.

Figure 1-1. Multilok High Speed Data Modem Model 6005
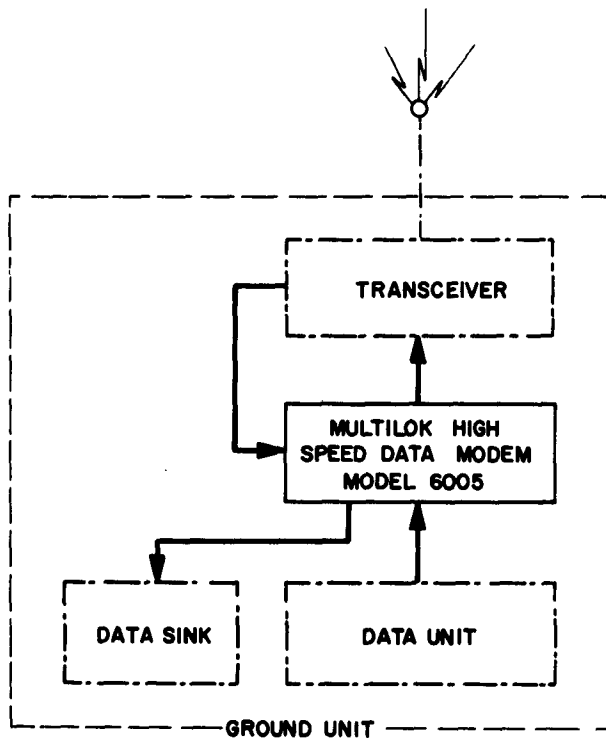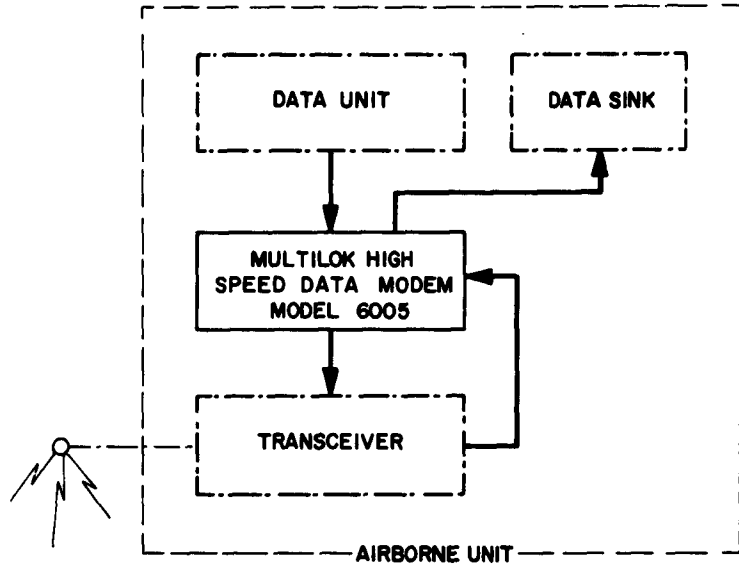
Figure 1-2. Multilok Data System

DEMODULATOR
CIRCUIT BOARD

DEMODULATOR
BAND PASS FILTER

IDLE SWITCH

MODULATOR
BAND PASS FILTER

MODULATOR
CIRCUIT BOARD

MODULATOR
BAND PASS FILTER
(CONVERTER NETWORK)

INTERCONNECTION
BOARD

LOW PASS FILTER

Q3
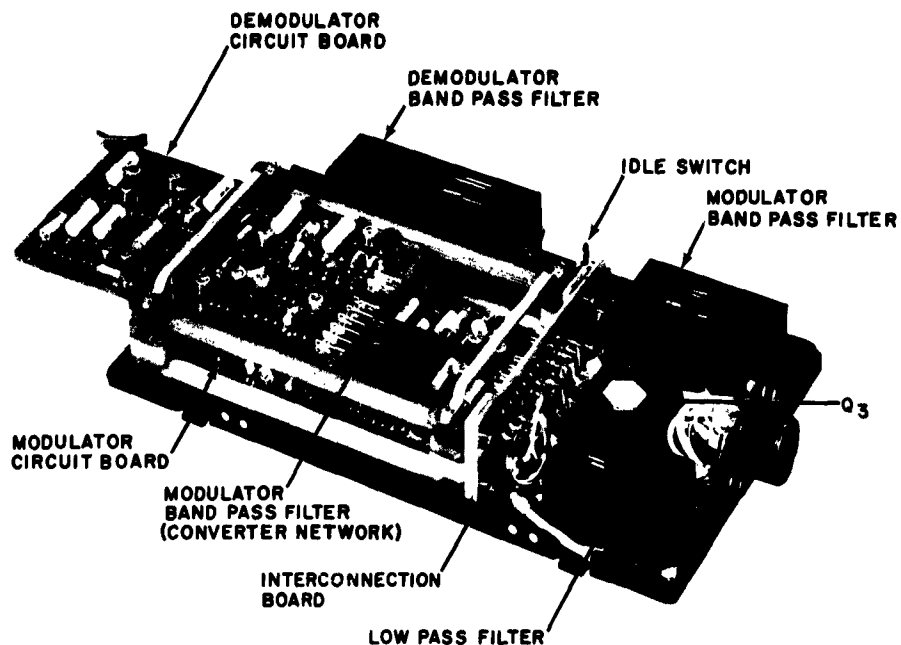
Figure 1-3. Multilok High Speed Data Modem Assemblies

The Multilok High Speed Data Modem operates by phase modulating a sinusoidal carrier (2400 cps) with digital intelligence and reconstructing this digital signal at the demodulator. Upon receipt of the modulated signal at the demodulator, it passes through amplitude limiters, a detector, and low pass filter at which time the modulating intelligence is in the form of alternating pulses. These pulses are then applied to a squaring circuit (Schmitt trigger) which in effect performs an integration to reconstruct the original digital modulating waveform.

Specifications for the Multilok High Speed Data Modem are listed in Table 1-1.

Table 1-1. Specifications.

Signal
    Transmission . . . . Phase-shifted audio tone (2.4 kc).
    Bandwidth. . . . . 1200 cps (1.8 to 3.0 kc)
    Data Rate . . . . 60 to 1200 bps, non return to zero, synchronized
                               to transmission carrier.

Environment
   Temperature
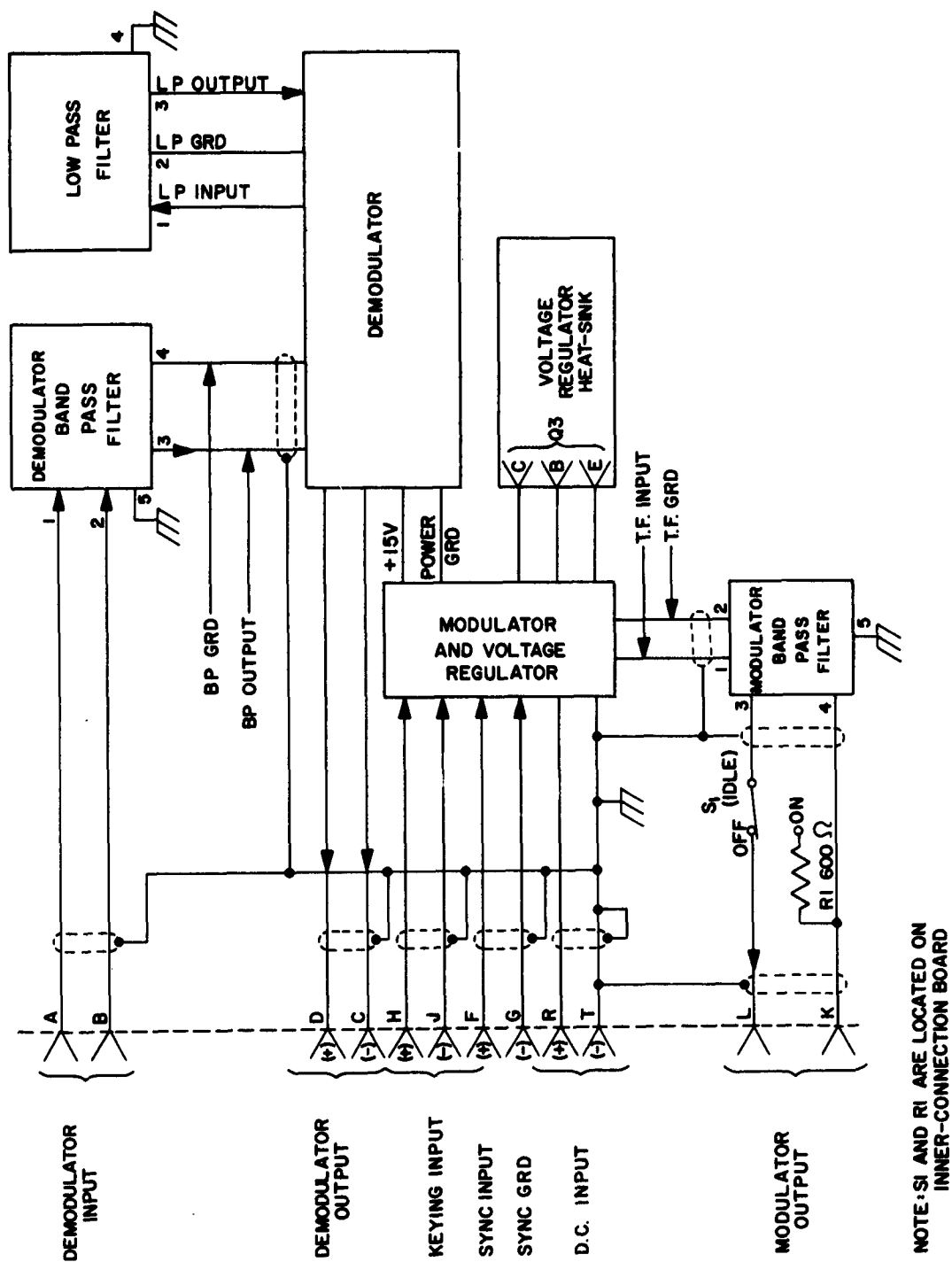
Figure 1-4. Multilok High Speed Data Modem Block Diagram

Operating	-10°C to 55°C
Storage.	-40°C to 85°C
Humidity.	0 to 95% Relative humidity

Mechanical

Size	12 in. Wide x 7 5/8 in. High x 2 1/4 in. Deep
Weight	6 lbs
Interface Connector	Cannon (19 pin) MS3102A-20-29P
Filters	4 Filters: Modulator Bandpass, Demodulator Bandpass, Demodulator Low Pass, Resonant Circuit (individually encased and sealed)
Circuit Boards.	2 Boards: Modulator-Voltage Regulator, Demodulator. Constructed on glass epoxy laminate.

Electrical

Power Requirements.	+27.5V dc +10%, -20% (+30.25V, +22V); 250 milliamps maximum; negative common ground.

Modulator

Input Keying Impedance . . .	10K Ohms
Input Keying Voltage	0V ±0.5V and +6V ±0.5V
Output Impedance	600 Ohms - Isolated, balanced.
Output Power Level	0 dbm ±1 db (adjustable)
Synchronizing Signal	Square or Sinusoidal, 2400 ±10 cps, 6V pp into 10K Ohms
Carrier	2400 cps

Demodulator

Input Impedance	600 Ohms - Isolated, balanced.
Input Power Level	0 dbm to -50 dbm
Output Impedance	50 Ohms
Output Voltage	0V and +6V

1.2 CIRCUIT DESCRIPTION.

1.2.1 MODULATOR.

The modulator converts dc non-return to zero (nrz) binary signals into a phase shifted carrier signal. This signal is then sent to the demodulator, via radio transmission, to be reconstructed into the original modulating intelligence. The modulator consists essentially of a synchronizer converter, keying network, amplifier, and modulator band pass filter. Figure 1-5 represents the modulator in block diagram form and figure 5-1 is the schematic diagram. All referenced test points and their locations are shown in figure 5-3. Each block will be treated individually in the description.

Figure 1-5. Modulator Block Diagram

1.2.1.1 EMITTER FOLLOWER. The emitter follower Q5 is used to provide a high impedance to the synchronizing signal and a low source impedance to the converter network. The impedance at the synchronizing input te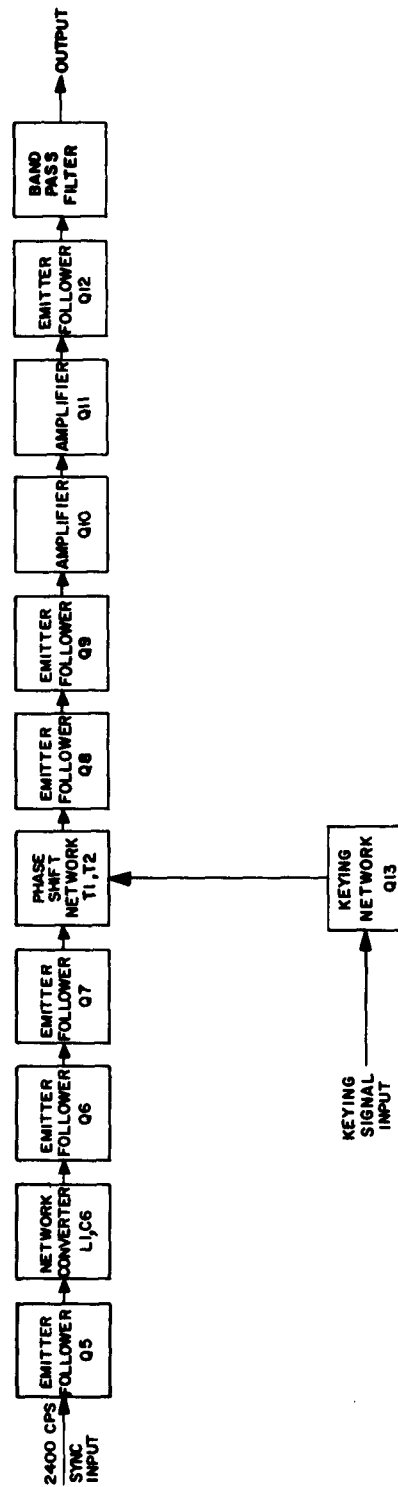rminal is approximately 10k ohms. Figure 1-6A represents a typical synchronizing signal and figure 1-6B represents the output of Q5 before application to the converter.

1.2.1.2 CONVERTER. The converter network (resonant circuit) is composed of inductor L1 and capacitor C6 encased in a metal container and mounted on the modulator circuit board. This network is designed to resonate at 2400 cps. Figure 1-7 indicates the amplitude response versus frequency of the converter network. The network has a resonant impedance of approximately 30k ohms and a Q greater than 40. Input impedance of the network is 600 ohms and output impedance is 22k ohms. The output of the converter will be sinusoidal with either a sine wave or square wave as the synchronizing input. This output is coupled by capacitor C7 and resistor R16 to emitter follower Q6.

1.2.1.3 EMITTER FOLLOWER. Emitter follower Q6, in conjunction with Q7, is used to provide a high input impedance for the converter network. The signal output at this point is sinusoidal and is now coupled into the phase shifting network by transformer T1. Figure 1-6C represents this output at TP4.

1.2.1.4 PHASE SHIFT NETWORK. The phase shift network is composed of transformer T2, capacitors C12 and C13, and diode bridge (switch) CR3 through CR6. The keying network, composed essentially of transistor Q13 and diodes CR7 through CR14, is also directly involved with the phase shift network, but will be discussed later.

The phase relationship of the 2400 cps carrier signal is determined by the effects of the R-L-C components in the phase shift network. When a positive going signal is applied to the keying input terminals, diodes CR3 through CR6 are forced into conduction. This presents a low impedance at the transformer terminals, which is reflected into the secondary of transformer T2 as a low impedance. This change of impedance in conjunction with C12 and C13 changes the degree of phase shift within the network. In the absence of the modulating signal, the diode bridge does not conduct, which presents a high impedance to the transformer. This high impedance is reflected to the secondary of T2 and this change of impedance in conjunction with C12 and C13 alteres the phase shift characteristics of the network. Therefore, two discrete changes in phase of the 2400 cps carrier signal result when the modulating signal is turned on and off.

Potentiometer R54 is utilized to compensate for any unbalance conditions that result due to variations of diodes CR3 through CR6. The phase shifted signal appears at the center arm of potentiometer R25 which is used as a balance adjustment. Proper adjustment of R25 is indicated by an equal amplitude signal after each phase shift transition. The phase shifted signal is then coupled to the next stage, emitter follower, by capacitor C14.
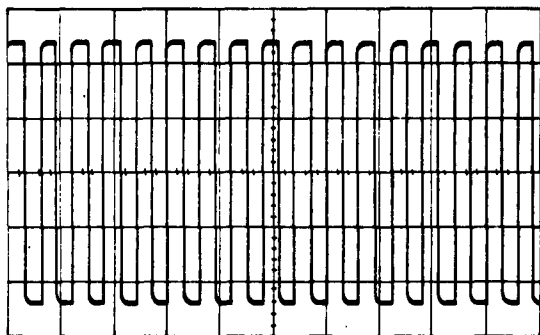
A. SYNC. SIGNAL INPUT-2400 CPS-6V P/P
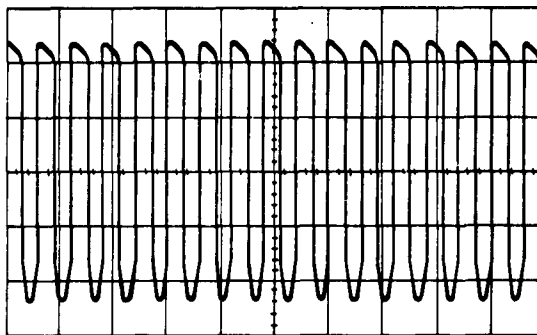
B. TP6 (OUTPUT Q5)-2400 CPS -2V P/P
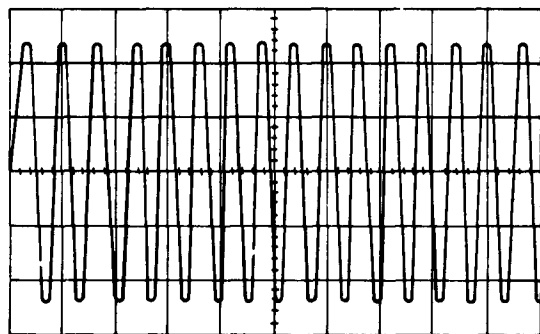
C. TP4 (OUTPUT Q 7) -2400 CPS CARRIER 3V P/P
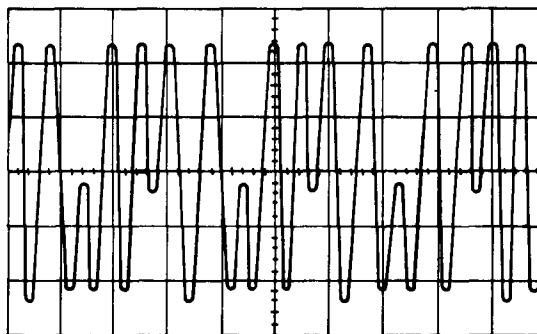
D. TP5 (OUTPUT Q9)   PHASE SHIFTED CARRIER
   MODULATED WITH 1200 BPS SQUARE WAVE 0.11 V P/P
   TPI (OUTPUT Q II) PHASE SHIFTED CARRIER 2.2VP/P
   TP2 (OUTPUT Q 12) PHASE SHIFTED CARRIER 2.2VP/P
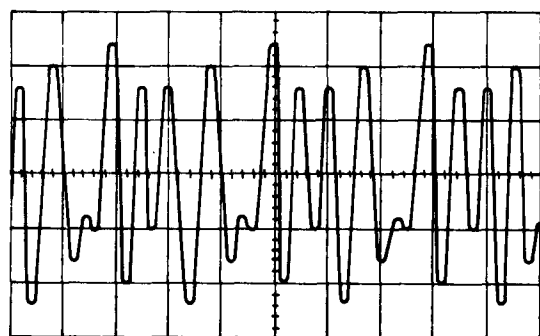
E. INPUT TO MODULATOR BAND PASS FILTER
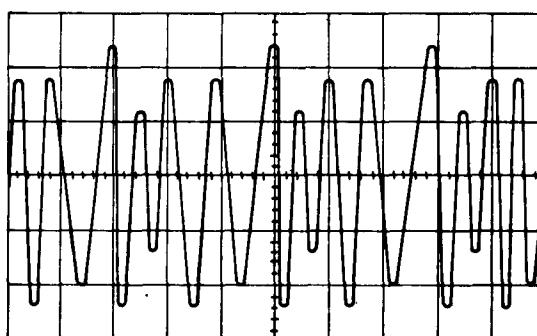
F. MODULATOR OUTPUT

Figure 1-6.   Modulator Waveforms

1-8
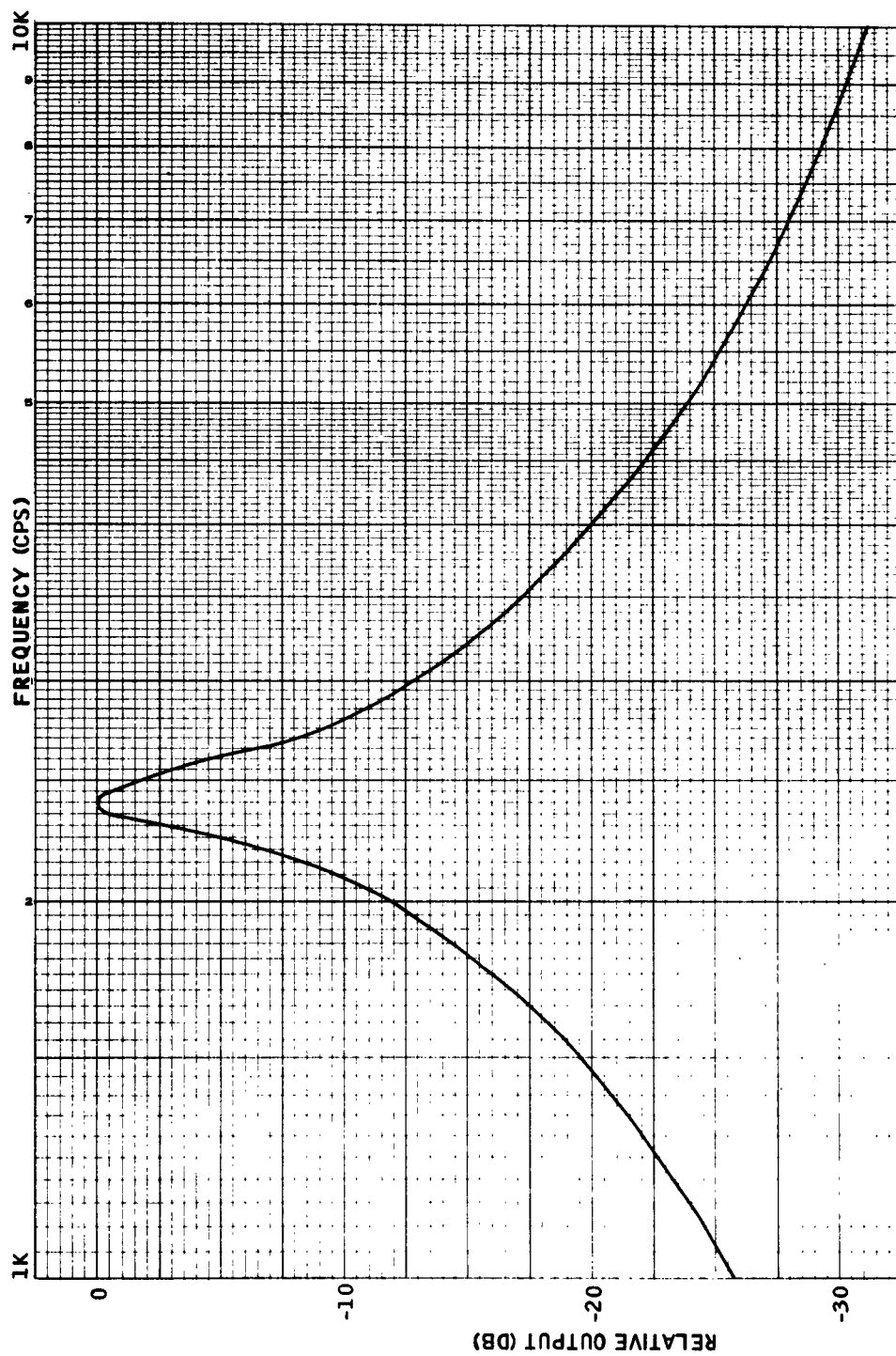
Figure 1-7. Resonant Circuit Amplitude Response Characteristic Curve

1.2.1.5 EMITTER FOLLOWER. Emitter follower Q8 and emitter follower Q9 are connected in a super alpha configuration to provide a high input impedance to the phase shift network as well as providing a low source impedance for the following variable gain amplifier stage. Figure 1-6D (TP5) shows the characteristic shape of the phase shifted signal, modulated with a 1200 bps square wave.

1.2.1.6 AMPLIFIER. The variable gain amplifier is comprised of transistors Q10 and Q11 providing a voltage gain in excess of 30 db. Gain of the amplifier is controlled by potentiometer R35. Figure 1-6D (TP1) depicts the output of this amplifier.

1.2.1.7 EMITTER FOLLOWER. Emitter follower Q12 is coupled to the amplifier by capacitor C17 and provides the required impedance match to the modulator band pass filter. Figure 1-6D (TP2) indicates the phase modulated signal at the output of Q12. This signal is then coupled to the modulator band pass filter by C18 and R46. C18 provides dc isolation and R46 provides the necessary source impedance for the filter.

1.2.1.8 MODULATOR BAND PASS FILTER. The modulator band pass filter is employed to pass only the phase modulated carrier signal and the first pair of sidebands. This prohibits spurious and unwanted frequencies from being transmitted on the line. The band width of this filter is approximately 1500 cycles at the 3 db attenuation point as indicated by the response curve in figure 4-4. Figure 5-5A is a schematic of the filter.

1.2.1.9 KEYING NETWORK. The keying network consists of transistor Q13, diodes CR7 through CR14, 8 resistors and one capacitor. These function to select a signal of approximately 1.1 volt pp out of the center of the input keying (modulating) waveform, which is approximately 6 volts pp. The output, 1.1 volts pp, is applied to the center arm of R54 of the balanced diode bridge (switch). Capacitor C20 integrates the output signal slightly to suppress transient noise at the keying transitions.

1.2.2 VOLTAGE REGULATOR.

The voltage regulator, mounted on the modulator circuit board, provides a regulated +15 volts dc to the modulator-demodulator circuits. Regulation is constant with input voltage variations between +22 volts dc and +30.25 volts dc. Figure 1-8 is a block diagram of the voltage regulator. Refer to figure 5-1 for the schematic diagram of the voltage regulator.

The reference voltage is derived from a 15 volt Zener diode, CR1. Regulation is provided by the series element transistor Q3, which is mounted on a separate heat sink attached to the chassis. With a constant load, the output voltage remains at +15 volts over the specified input voltage range.

When the input voltage increases above the steady state level, the voltage drop across R5 increases which makes transistor Q4 conduct more current. This in
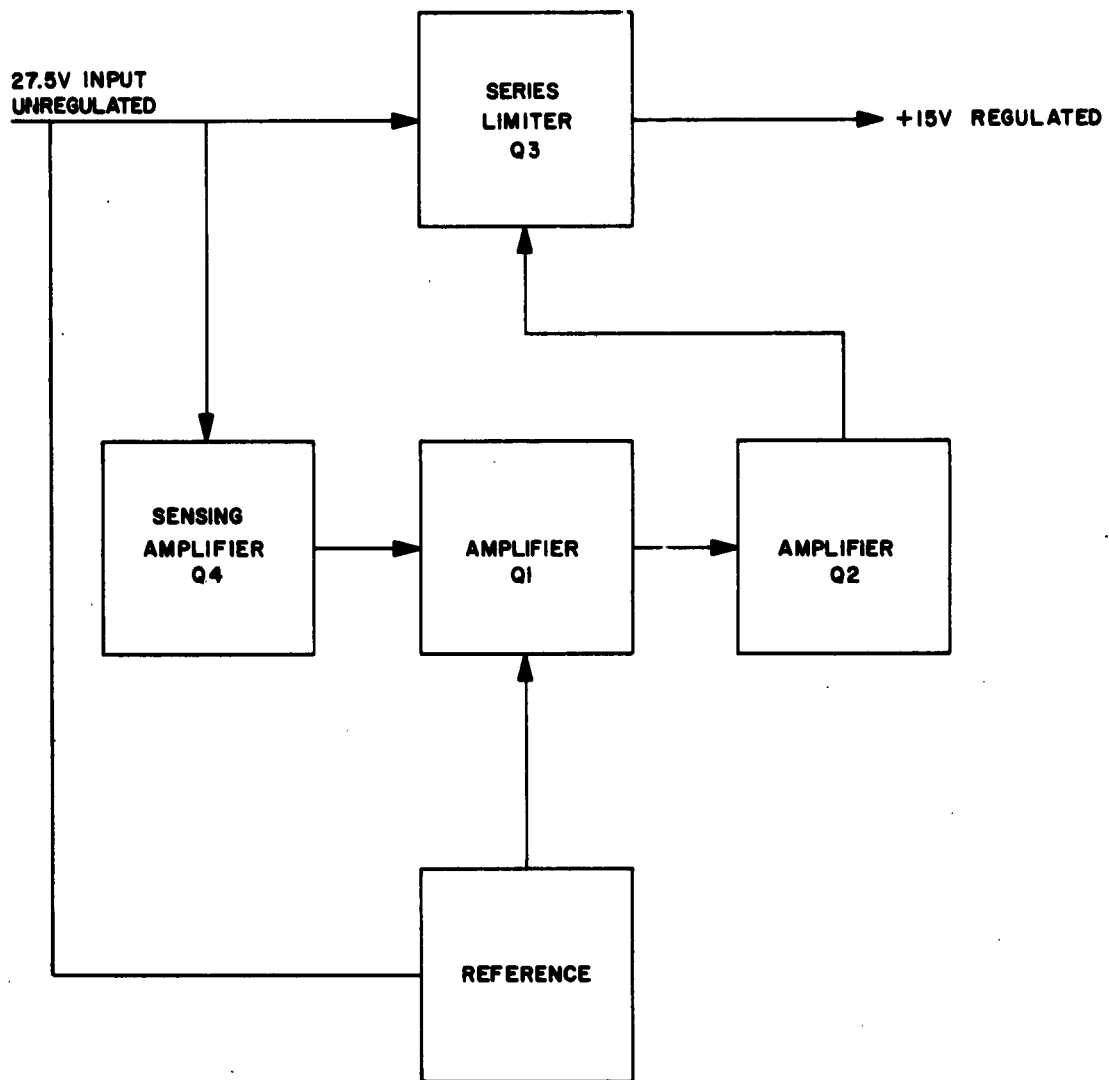
Figure 1-8.   Voltage Regulator Block Diagram

turn raises the voltage at the collector of Q4 and likewise at the base of Q1. Q1 then conducts less which reduces the base drive at Q2 causing Q2 to conduct less. Consequently, less base current drive is applied to Q3, which reduces the conduction of Q3 thus compensating for the increase of input voltage and maintaining the +15 volt output.

The opposite condition occurs when the input voltage drops below a steady state level. In this case, the voltage drop across R5 decreases, which reduces the base current drive to transistor Q4. This in turn lowers the voltage at the collector of Q4 and at the base of Q1. Transistor Q1 now conducts more current forcing Q2 into conduction. This yields more base drive current to transistor Q3 which causes Q3 to conduct more current, thus compensating for the decreased voltage and maintaining the +15 volt output.

1.2.3 DEMODULATOR.

The demodulator receives phase modulated signals from a radio receiver such as Bendix RA-18C. These signals, when reconstructed, forms dc intelligence equivalent to the original modulating intelligence. The demodulator is composed essentially of the following elements: band pass filter, limiter amplifiers, Schmitt trigger, detector, low pass filter, and Schmitt trigger for dc restoration (figure 5-2). Figure 1-9 represents the demodulator in block diagram form. Each block will be treated individually in the description. All referenced test points and their locations are shown in figure 5-4.

1.2.3.1 DEMODULATOR BAND PASS FILTER. The demodulator band pass filter is used to limit the band width of the incoming modulated signal and attenuate all undesired frequencies. The bandwidth is approximately 1300 cycles at the 3 db attenuation point as indicated by the response curve in figure 4-5. Figures 1-6A and 1-6B represent the input and output signal waveforms of the phase modulated carrier. The filter schematic appears in figure 5-5B.

1.2.3.2 EMITTER FOLLOWER. Emitter follower Q1 is coupled to the modulator band pass filter output by capacitor C1. The emitter follower is used to obtain the desired impedance match of the band pass filter and provide a low source impedance for the amplitude limiter.

1.2.3.3 AMPLITUDE LIMITER. The amplitude limiter Q2 functions to limit the amplitude of the signal to approximately 1 volt pp. Limiting is accomplished by diodes CR1 and CR2 providing negative feedback to the base of Q2 when the diodes are in conduction. CR1 conducts when the ac amplitude at the collector reaches the forward conduction voltage drop of the diode, or approximately minus 0.5 volts. Likewise, CR2 conducts when the ac signal voltage at the collector reaches the forward conduction voltage drop of the diode, or approximately positive 0.5 volts. The output thus approaches a square wave with an amplitude equal to the voltage drop across the diodes during conduction. Figure 1-10C represents the output at TP2 (Q2). Output of Q2 drives a similar amplitude limiter Q3. The action of this

1-12

/
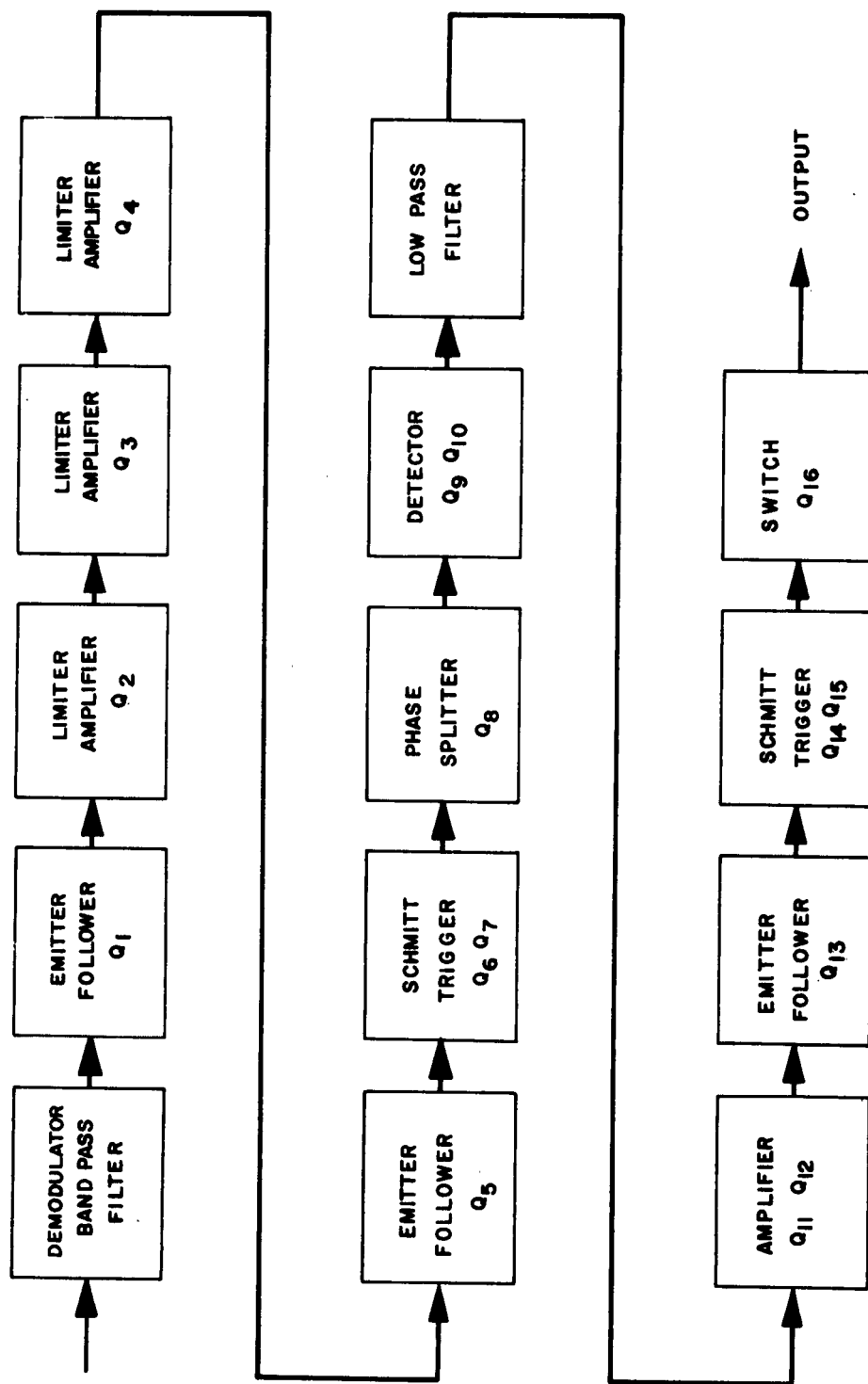
Figure 1-9. Demodulator Block Diagram
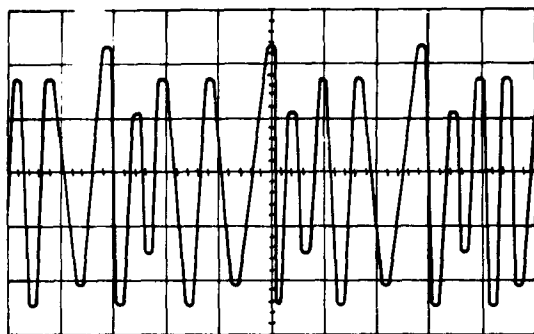
A. DEMODULATOR INPUT
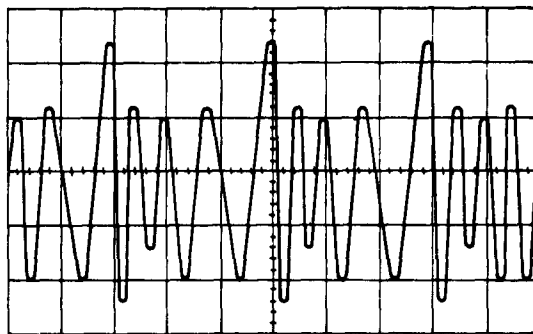
B. TP I BAND PASS FILTER OUTPUT
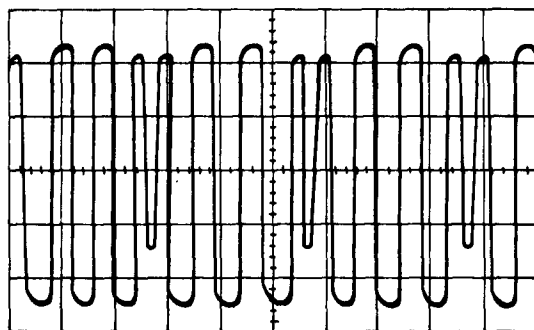
C. TP2 (OUTPUT Q2) LIMITER NO. I-IV P/P
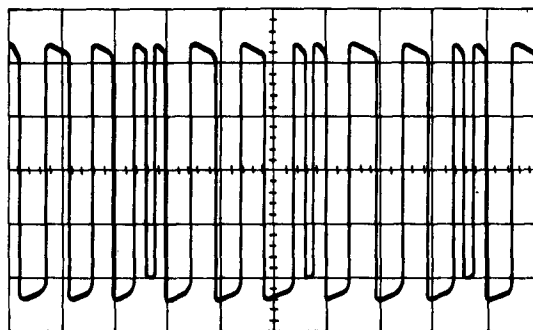
D. TP3 (OUTPUTQ3) LIMITER NO.2- 1V P/P
   TP4 (OUTPUTQ4) LIMITER NO.3- 2 V P/P
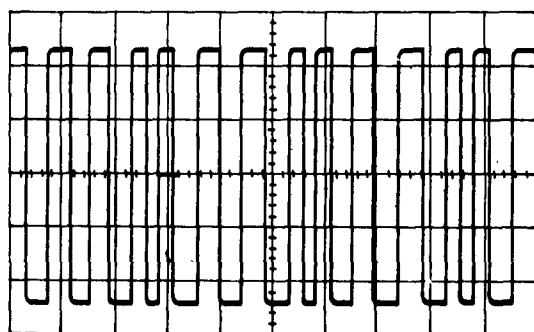
E. TPI (OUTPUT Q7) SCHMITT TRIGGER-6V P/P
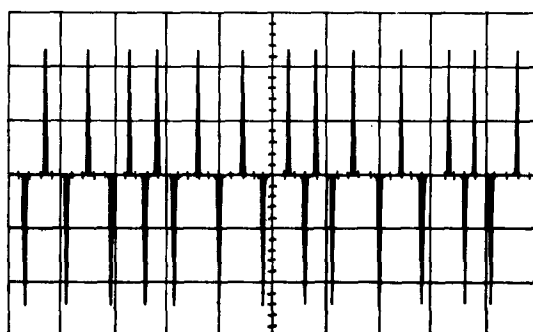
F. BASE Q8

Figure 1-10. Demodulator Waveforms - 1200 BPS Square Wave
Modulating Signal (Sheet 1 of 2)
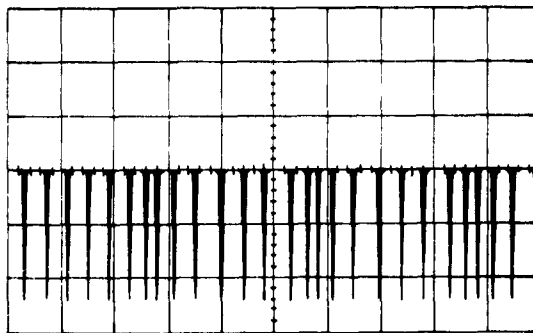
G. TP6 RECTIFIED
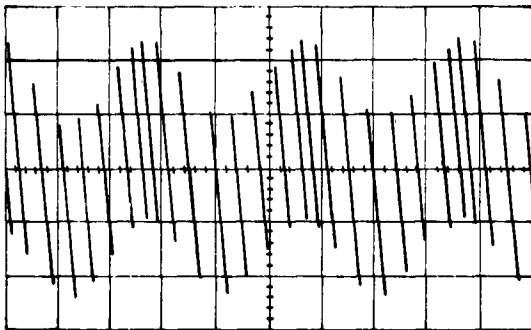
H. LOW PASS FILTER INPUT
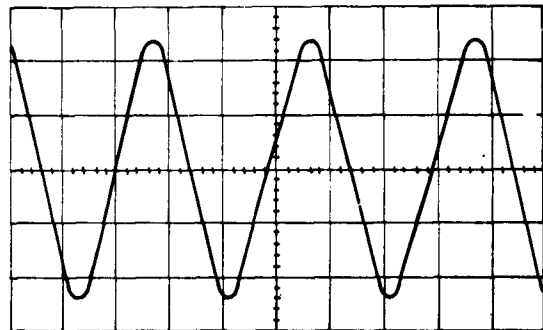
I. TP 7 (OUTPUT Q 12) AMPLIFIED LOW PASS FILTER
OUTPUT -4.3 V P/ P

TRIGGER POINTS
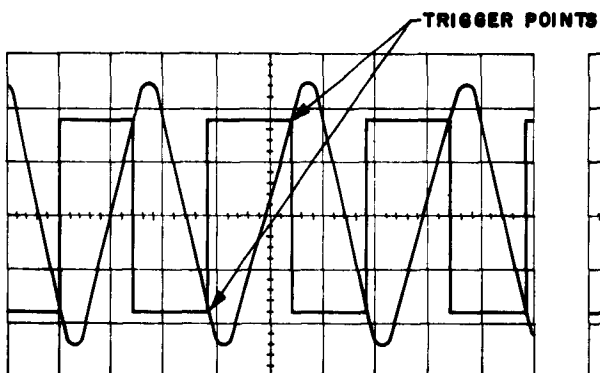
J. T.P7 & TP9 – RELATIONSHIP OF LOW PASS
VERSUS SCHMITT TRIGGER OUTPUT
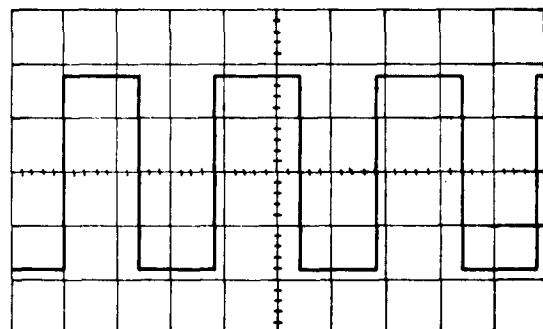
K. DEMODULATOR OUTPUT - 6V P/ P

Figure 1-10. Demodulator Waveforms - 1200 BPS Square Wave
Modulating Signal (Sheet 2 of 2)

limiter is identical to that described above producing a square wave output with steeper wavefronts. Figure 1-10D represents the output at TP3 (Q3). This output is fed into another amplitude limiter Q4. The operation of Q4 is identical to the previous limiter with the exception that there are two diodes, in series, in each branch. The output amplitude is thus limited to approximately 2 volts pp, or the forward voltage drop across the diodes when in conduction. CR5-CR6 conduct when the ac signal is about 1.0 volt negative and CR7-CR8 conduct when the signal is about 1.0 volt positive. Figure 1-10D represents the output at TP4 (Q4). The output of Q4 is then coupled to an emitter follower Q5 which provides a low source impedance to the next stage, Schmitt trigger.

1.2.3.4 SCHMITT TRIGGER. The Schmitt trigger circuit Q6 and Q7 is driven by a signal equal to that from Q4. As the input to Q6 goes positive, Q6 will turn on at some positive voltage set by the bias points of the circuit, and Q7 will turn off by regenerative action. The output at the voltage divider R28-R29 will thus go positive, approaching +15V at the limit. Conversely, Q6 will turn off as the input signal reaches a preset negative voltage and Q7 will turn on by regenerative action. The output will now go negative approaching about +9 volts as the lower limit. The combined output is a square wave with 6V pp swing with constant rise and fall times. Figure 1-10E indicates the output at TP5 (Q7). Operation of the Schmitt trigger ceases when the line level into the demodulator is lower than -50 dbm. At this point the amplitude of the signal from the amplitude limiter is too low to operate the Schmitt circuit.

1.2.3.5 PHASE SPLITTER. The phase splitter Q8 receives its input from the Schmitt trigger through capacitor C13. C13 in combination with R31 and R32 takes the form of a differentiator, whose RC time constant is much less than the period of the signal input. Differentiating a square wave results in positive and negative going pulses, "spikes," with respect to the input. Figure 1-10F indicates this signal which appears at the base input of Q8. The phase splitter produces two outputs equal in amplitude and opposite in phase. The chain of positive and negative pulses from each output is coupled through C14 and C15 respectively and rectified by CR9 and CR10.

The resulting output at TP6, figure 1-10G, is a chain of negative pulses with a repetition rate equal to twice the original carrier frequency. These pulses are representative of the zero axis crossings of the phase modulated signal. R38 is provided to adjust the pulses for equal amplitude, and compensate for amplitude differences of the negative pulses due to variations of diodes CR9 and CR10. The negative pulses are then coupled directly to the amplifier-detector stage.

1.2.3.6 AMPLIFIER - DETECTOR. Transistor Q9 operates as a saturated dc coupled amplifier, normally biased in the "on" condition. This amplified output is then directly coupled to the detector, Q10. The resulting amplified pulses are representative of the zero axis crossings of the phase modulated carrier signal. In the absence of a modulating signal, the zero axis crossing time intervals are equal since the carrier is not shifted in phase. When a modulating signal is applied,

1-16

the time intervals between adjacent zero axis crossings of the carrier are modified during the time of the phase transition. The pulses at the input to the detector represents this time interval change in the axis crossings.

The detector produces either a positive or negative signal output for each phase transition of the carrier signal and a steady level for the time between transitions or in the absence of a modulating signal. If the modulating signal advances the phase, thus increasing the number of pulses per unit time to the detector, capacitor C16 charges above the quiescent level resulting in a positive output voltage. Likewise when the phase is retarded the number of pulses per unit time during the phase transition is reduced thus causing capacitor C16 to loose some charge resulting in a voltage lower than the quiescent. The overall result is a series of positive and negative going signals representative of an amplitude modulated signal containing the binary intelligence. This signal, figure 1-10H, is coupled to the demodulator low pass filter through capacitor C17. C17 is provided for dc isolation of the low pass filter.

1.2.3.7 LOW PASS FILTER. The low pass filter is used to remove all high frequency components from the detected waveform and pass only the low frequencies, which represent the modulating signal. Frequency response of this filter is limited to approximately 600 cps at 3 db attenuation as shown by the amplitude response in figure 1-11. Figure 5-5C is a schematic diagram of the filter.

1.2.3.8 AMPLIFIER. The amplifier, coupled directly to the low pass filter output, is composed of transistors Q11 and Q12. This amplifier is designed to provide the necessary matching impedance for the low pass filter and provides approximately 20 db voltage gain. Figure 1-10I is representative of the amplifier output at TP7.

1.2.3.9 EMITTER FOLLOWER. The emitter follower Q13 is used to provide a low source impedance for driving the next stage, Schmitt trigger. Potentiometer R52 provides a means of adjusting the gain of the signal into the Schmitt trigger.

1.2.3.10 SCHMITT TRIGGER. The Schmitt trigger, composed of transistors Q14 and Q15, is the final step in the reconstruction process of the original modulating intelligence. The amplified signal from the low pass filter is applied at the base of Q14. When the signal at Q14 goes positive, Q14 will turn on and Q15 will turn off by regenerative action. The output from Q15 in this state is approximately +10 volts and represents a positive change of state of the digital modulating signal. When the input at Q14 is negative, Q14 is forced to turn off and Q15 turns on. The output is now approximately +2 volts and represents a negative change of state of the modulating signal.

The "trigger" points are adjustable by means of R54 (bias) and R52 (gain). The trigger points are set to occur at approximately 50% of the positive and negative excursion of the input signal. Figure 1-10J indicates this cross over point in relation to the Schmitt trigger output.
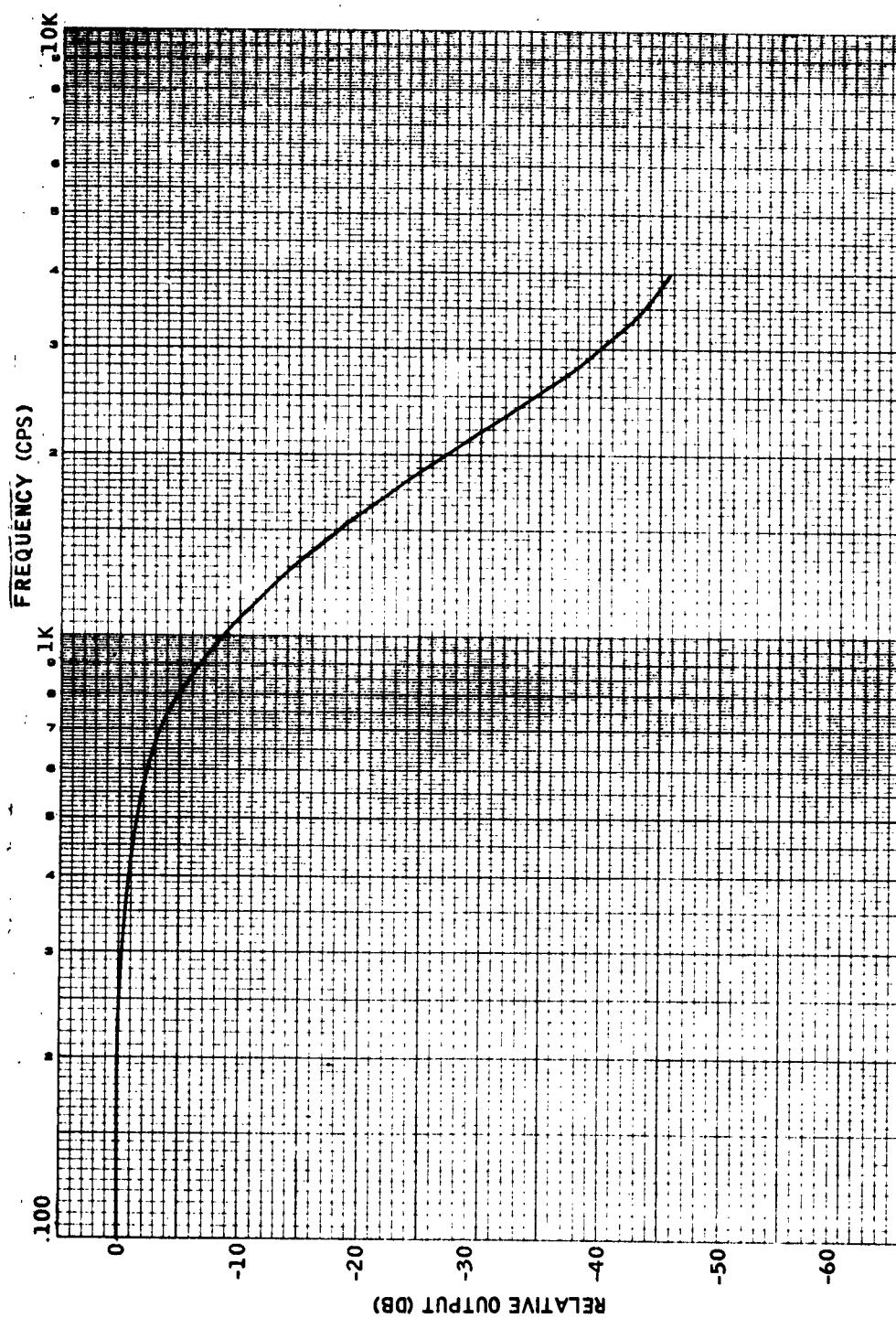
Figure 1-11.   Low Pass Filter Amplitude Response Characteristic Curve

1.2.3.11 EMITTER FOLLOWER. The emitter follower Q16 provides the required 0V and +6V output signal. Q16 is coupled to the Schmitt trigger output by diodes CR12 through CR17, which provide the necessary voltage drop to cause Q16 to be turned off when the Schmitt trigger output is low, +2V. Q16 is turned on when the Schmitt trigger output is high, +10V, and provides an output of +6V as set by the zener diode CR18. Figure 1-10K indicates the output of the demodulator.

SECTION II

MAINTENANCE

2.1 MAINTENANCE

Maintenance described in this section shall be restricted primarily to adjustments on either the modulator or demodulator. Referenced figures will be used to indicate appropriate waveforms in relation to adjustments.

2.1.1 TEST EQUIPMENT

Test equipment required for maintenance is listed in table 2-1.

Table 2-1. Test Equipment.

VTVM	Hewlett-Packard Model 400D (or equivalent)
Oscilloscope	Tektronix Model 535 with Type CA plug in unit (or equivalent)

2.1.2 MODULATOR

Three adjustments are provided on the modulator circuit board.

a. DC balance R54
b. AC balance R25
c. Gain adjust R35

Apply a binary signal with 0 and +6 volt levels to the keying input terminals at a rate of 1200 bits per second. Observe TP5 with an oscilloscope with sweep adjusted to view at least three transitions of the shifted signal. Adjust R25 for equal amplitude of each section of the shifted signal. Adjust R54 to align each section if they appear to be displaced from each other. Figure 1-6D indicates the signal form after proper adjustment.

The signal output level of the modulator is adjusted by R35. Connect a VTVM across the 600-ohm resistor (R1) located on the interconnecting circuit board. Disconnect modulating signal. Set idle switch S1 on interconnecting circuit board to on. Adjust R35 for desired output level in dbm. Return S1 to the off position for system operation. No other adjustments are necessary for operation of the modulator.

2.1.3 DEMODULATOR

Three adjustments are provided on the demodulator circuit board.

a. Phase splitter balance R38
b. Schmitt trigger gain adjustment R52
c. Schmitt trigger bias adjustment R54

Connect a phase modulated signal (modulator output) to the signal input terminals of the demodulator. With modulation off (carrier only), check level of signal with VTVM at the demodulator input terminals. The level should be between 0 and -50 dbm.

Connect the oscilloscope input to TP6. Adjust oscilloscope to view the negative portion of the pulses. Adjust R38 to obtain equal pulse amplitude, figure 1-10G.

With modulation applied (1200 bps square wave), connect one input of oscillopscope to TP7. Connect the second input to TP9. Adjust the oscilloscope to obtain a trace that takes the form of a sine wave from TP7.

Set R52 for maximum gain, fully counterclockwise. Adjust R54 until a symmetrical square-wave pattern is observed at TP9. Superimpose the two traces and observe the point where triggering occurs in relation to the trace at TP7. The trigger points, leading and trailing edges of the square wave output, should be approximately half way between the zero axis crossing and peak points of the signal at TP7. Too much signal gain, as determined by setting of R52, into the Schmitt trigger circuit will cause the trigger points to be nearer the zero axis crossing while too little gain will force the trigger points near the peaks of the signal from TP7. Adjust R52 in conjunction with R54 until the trigger points are approximately half way and the resultant square wave output is symmetrical. Figure 1-10K indicates how these signals look when properly adjusted.

SECTION III

DESIGN THEORY

3.1 TECHNICAL CONSIDERATIONS

A fundamental consideration in a binary-phase-modulated communications systems is the magnitude of the phase shift of the carrier. For a sinusoidal modulating signal and sinusoidal carrier, phase modulation produces a frequency spectrum consisting of the carrier and pairs of sidebands for each integral harmonic of the modulation. The magnitudes of the sidebands are given by Bessel functions of the first kind with arguments equal to the phase shift (in radians) and order equal to the sideband harmonic number, viz.: the carrier amplitude is proportional to $J_0 (\Delta \ominus)$, each of the fundamental-modulation sidebands is proportional to $J_1 (\Delta \ominus)$, etc. [1]

Applying this information to the particular case at hand (square wave modulation) is accomplished by remembering that a square wave is a Fourier series of odd harmonic sinusoids. Hence, each harmonic of the fundamental modulating frequency has its own spectrum similar to that outlined above. Therefore, an optimum angle based on the above simplified mathematical treatment should also be near the optimum value for square wave keying.

The criterion used to choose the optimum angle is that maximum power should be generated in the first pair of sidebands compared to all other sidebands including the unkeyed carrier component. Higher order sidebands than the first are not passed by the filters, and can not contribute to intelligence at the demodulator. Likewise, the component which is the unkeyed carrier (0th order), even though it is passed by the filters, by definition does not contribute to information at the demodulator. A plot of Bessel functions of the first kind will show that an argument just less than 2.0 will best fulfill the above optimum requirements. [2] The actual crossover for J_0 and J_2 is at approximately 1.86. [3] This corresponds to a keying angle of 1.86 radians or 106.5 degrees.

The above discussion also partially explains the changed envelope of the keyed carrier after it passes through a filter. Chopping off sidebands will inevitably generate A.M. on the carrier, because of the vector addition of the various sidebands. [4] A contributing cause of the rounding of the carrier envelope is the finite delay time in the band pass filter. The filter contains energy storage elements (capacitors and inductors) and therefore requires a finite time to pass intelligence. The abrupt phase changes of the incoming carrier are slowed and smoothed by the filter storage such that the phase changes in the outgoing carrier reach equilibrium in several carrier cycles rather than in less than one cycle.

(.1) Hund, August, _Frequency Modulation_, McGraw-Hill, 1942, pp. 16-28.

(2) Terman, Frederick E. , _Electronic and Radio Engineering_, McGraw-Hill, 1955, p. 590.

(3) _Reference Data for Radio Engineers_, Fourth Edition, International Telephone & Telegraph Corporation, 1956, pp. 1118-1120.

(4) Hund, August, _Frequency Modulation_, McGraw-Hill, 1942, pp. 90-92.

SECTION IV

ACCEPTANCE TEST REPORT

4.1 GENERAL.

This section contains information and data relative to the acceptance test performed at Robertshaw-Fulton Controls Company at Anaheim, California for the Federal Aviation Agency on the Multilok High Speed Data Modems Model 6005.

The acceptance test procedure consisted of six parts. These were: Dynamic Range, Error Rate, Power Supply Variation, Data Rate, Filter Bandwidth and Phase Characteristics of the simulated 600 ohm transmission line. All operations were performed at the time of acceptance test, except Filter Bandwidth and the transmission line Phase Characteristic. Filter Bandwidth was recorded at the time of filter assembly and transmission line Phase Characteristics were determined prior to the acceptance test. These curves are included as part of this report.

4.2 TEST PROCEDURE DESCRIPTION.

4.2.1 DYNAMIC RANGE.

Dynamic range of the Multilok 6005 Demodulator shall be measured using the test setup shown in Figure 4-1. The circled numbers correspond to test equipment used which is listed in table 4-5.

The signal amplitude at the input of the demodulator shall be reduced from 0 dbm to -50 dbm without deterioration of the signal at the output of the demodulator. Signal amplitude to the demodulator is controlled by the gain control on the amplifier (Item #5) with a signal level of 0 dbm from the modulator.

Monitor errors from the demodulator while modulating at a rate of 1200 bits per second (random signal pattern). Continue to reduce signal level to determine level where errors begin to occur. Resultant data is recorded in table 4-1.

4.2.2 ERROR RATE.

Error rate versus signal to noise ratio shall be determined utilizing the test setup shown in Figure 4-1.

With a signal level of -10 dbm into the demodulator, a signal to noise ratio of 30, 24, 18, 15 and 12 db shall yield an error rate not to exceed one error in 10^5 bits. Record error rate for signal to noise ratio of 9, 6, and 0 db.

Signal to noise ratios are to be measured on the 600 ohm line with no modulating signal. The frequency response of the line is restricted to a nominal 3 kc bandwidth as shown in Figure 4-2. Resultant data is recorded in table 4-2.

4.2.3 POWER SUPPLY VARIATION.

This test shall be performed using the test setup as shown in Figure 4-1. The system shall be operated at 1200 bits per second (random signal pattern) and a signal to noise ratio of 12 db. The power supply shall be varied between 20% below and 10% above the nominal value of 27.5 volts dc (22 to 30.25 volts dc respectively). The error rate shall not exceed one in 10^5 bits. Resultant data is recorded in table 4-3.

4.2.4 DATA RATE.

The test shall be performed using the test setup shown in Figure 4-1. The system shall be operated with a signal to noise ratio of 12 db. Modulating data rate shall be varied from 37.5 to 1200 bits per second (random signal pattern) in increments of 37.5×2^n where n is integers from 0 to 5.

The error rate shall not exceed one in 10^5 bits. Resultant data is recorded in table 4-4.

4.2.5 FILTER BANDWIDTH.

Bandwidth of modulator and demodulator band pass filters shall be determined from static filter response derived from test setup shown in Figure 4-3. These curves are shown in Figures 4-4 and 4-5.

4.2.6 PHASE CHARACTERISTIC CURVE.

The phase characteristic curve of the simulated line was determined using the test setup shown in Figure 4-6. The characteristic curve is plotted in Figure 4-7.

Table 4-1. Dynamic Range Test

Serial Number	Demodulator Signal Level (dbm)	Error In 10^5 Bits		Remarks
		Allowed	Actual	
1	0	0	0	Lower limit to deter-
	-50	0	0	mine where errors
	-60	-	1	begin to occur.
2	0	0	0	Lower limit to deter-
	-50	0	0	mine where errors
	-60	-	0	begin to occur.
	-61	-	1	

3	0	0	0	Lower limit to deter-
	-50	0	0	mine where errors
	-57	-	9	begin to occur.
	-60	-	2362	

Table 4-2. Error Rate Test

Serial Number	Signal to Noise Ratio in db	Errors in 10^5 Bits		Remarks
		Allowed	Actual	
1	30	0	0	S/N ratio of 12 db
	24	0	0	measured with Ballan-
	18	0	0	tine 320 VTVM yielded
	15	0	0	13 in 10^5 bits.
	12	1	19	Phase shift capacitor
	9	-	1,075	C13 changed to 3600
	6	-	11,145	uuf prior to start of
	3	-	28,094	test.
	0	-	39,822	
2	30	0	0	S/N ratio of 12 db
	24	0	0	measured with Ballan-
	18	0	0	tine 320 VTVM yielded
	15	0	0	106 errors in 10^5 bits.
	12	1	150	Phase shift capacitor
	9	-	1,453	C13 changed to 3600
	6	-	13,109	uuf. S/N ratio meas-
	3	-	29,984	ured with Ballantine
	0	-	40,222	320 VTVM now yielded
				16 errors. 22 errors
				counted when S/N ratio
				of 12 db was set with
				average reading VTVM.
3	30	0	0	S/N ratio of 12 db and
	24	0	0	9 db measured with
	18	0	0	Ballantine 320 VTVM
	15	0	0	gave 11 and 984 errors
	12	1	88	respectively.
	9	-	1,806	Phase shift capacitor
	6	-	14,879	C13 changed to 3600
	3	-	31,246	uuf prior to start of
	0	-	40,013	test.

Table 4-3. Power Supply Variation Test

Serial Number	Power Supply Voltage - Volts	Errors in 10^5 Bits		Remarks
		Allowed	Actual	
1	30.25	1	19	S/N ratio of 12 db
	27.5	1	9	measured with average
	22.0	1	18	reading VTVM.
2	30.25	1	14	S/N ratio of 12 db
	27.5	1	12	measured with average
	22.0	1	14	reading VTVM.
3	30.25	1	52	S/N ratio of 12 db
	27.5	1	88	measured with average
	22.0	1	78	reading VTVM.

Table 4-4. Data Rate Test

Serial Number	Data Rate Bits Per Second	Errors in 10^5 Bits		Remarks
		Allowed	Actual	
1	1200	1	9	Tests were conducted
	600	1	14	with a S/N of 12 db
	300	1	7	measured with a RMS
	150	1	72	VTVM. Power supply
	75	1	58	voltage at 27.5 volts dc
				1200 bits per second
				data rate taken from
				test (Table 4-3).
2	1200	1	12	Tests were conducted
	600	1	42	with a S/N of 12 db
	300	1	12	measured with a RMS
	150	1	22	VTVM. Power supply
	75	1	39	voltage at 27.5 volts dc
				1200 bits per second
				data rate taken from
				test (Table 4-3).
3	1200	1	88	Tests were conducted
	600	1	110	with a S/N of 12 db
	300	1	164	measured with a RMS
	150	1	335	VTVM. Power supply
	75	1	197	voltage at 27.5 volts dc
				1200 bits per second
				data rate taken from
				test (Table 4-3).

Table 4-5. Test Equipment

| Item No.	Description	Identification No.
1	Oscillator - H.P. Model 202 B	E-682
2	Random Noise Generator - H.H. Scbtt Model 811 B	E-132
3	Filter - Allison Model 2A	E-498
4	VTVM - Ballantine Model 300	E-804
4A	VTVM, True Reading RMS - Ballantine Model 320	E-359
5	Unit Amplifier General Radio Model 1206-B	E-205
6	Electronic Counter - H.P. Model 521-C	E-918
7	Electronic Counter - H.P. Model 521-C	E-926
8	Power Supply - H.P. Model 721-A	7789
9	Oscilloscope - H.P. Model 150A	E-320
10	VTVM - H.P. Model 400D	E-316
11	Random Sequence Generator - Robertshaw	
12	Mixer Amplifier - Robertshaw	
13	Bit Comparator - Robertshaw	
14	Unit Amplifier General Radio Model 1206B	E-474
15	Phase Meter - Advance Electronics Type 405	E-368
16	Oscillator - H.P. Model 200 AB	E-379
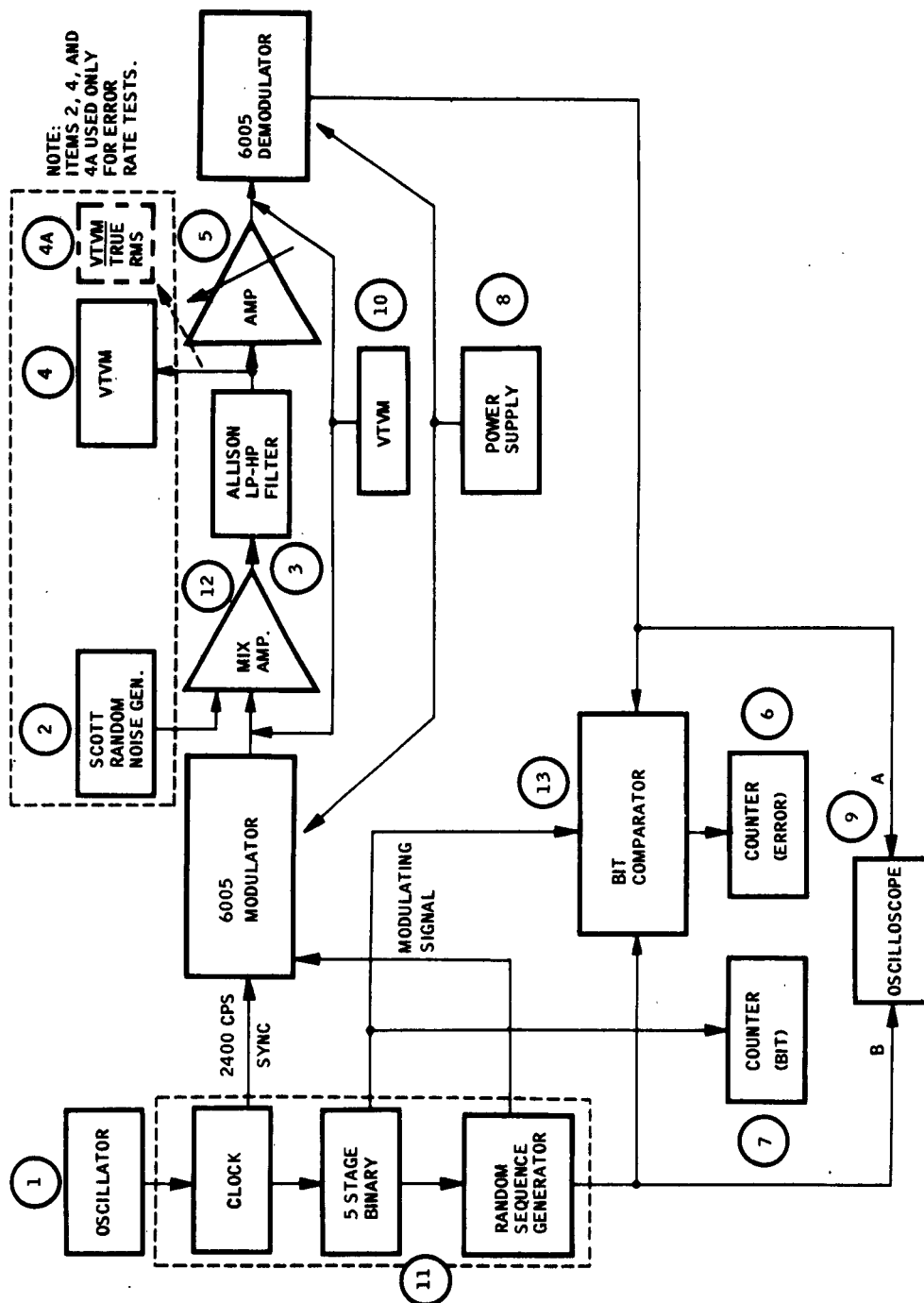
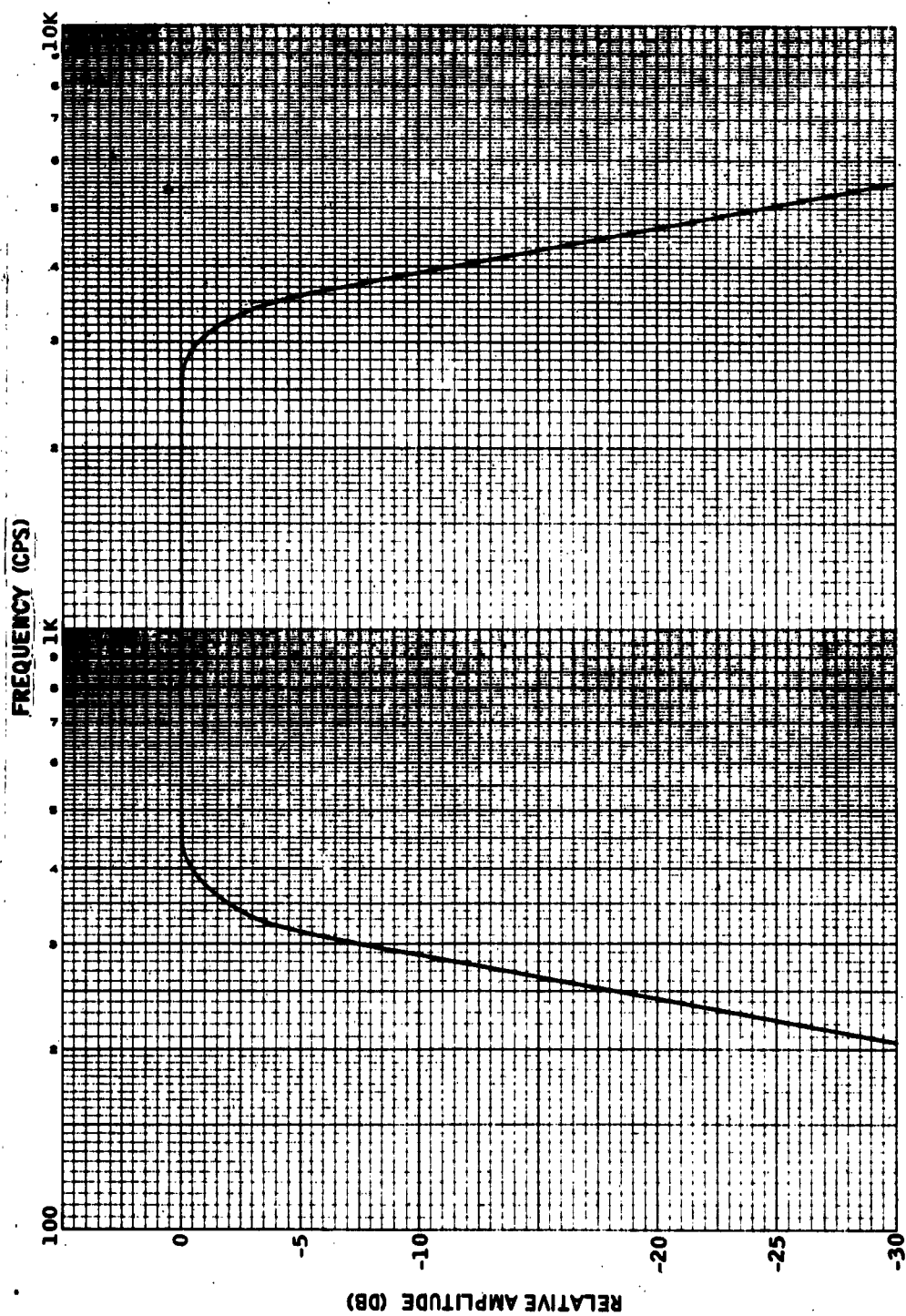Figure 4-1. Test Setup for Measuring Dynamic Range and Error Rates
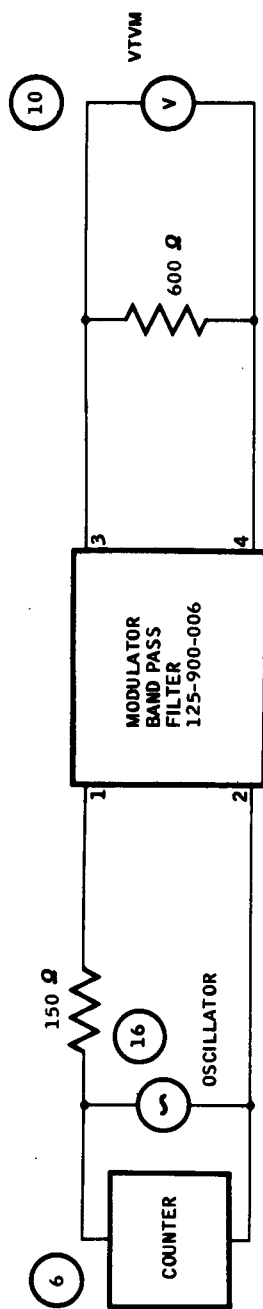
Figure 4-2. Frequency Response Curve of Simulated 600 Ohm Transmission Line
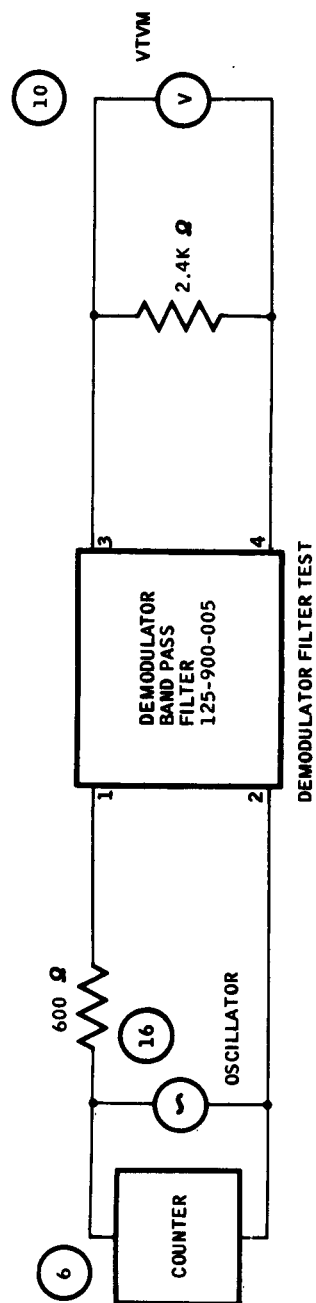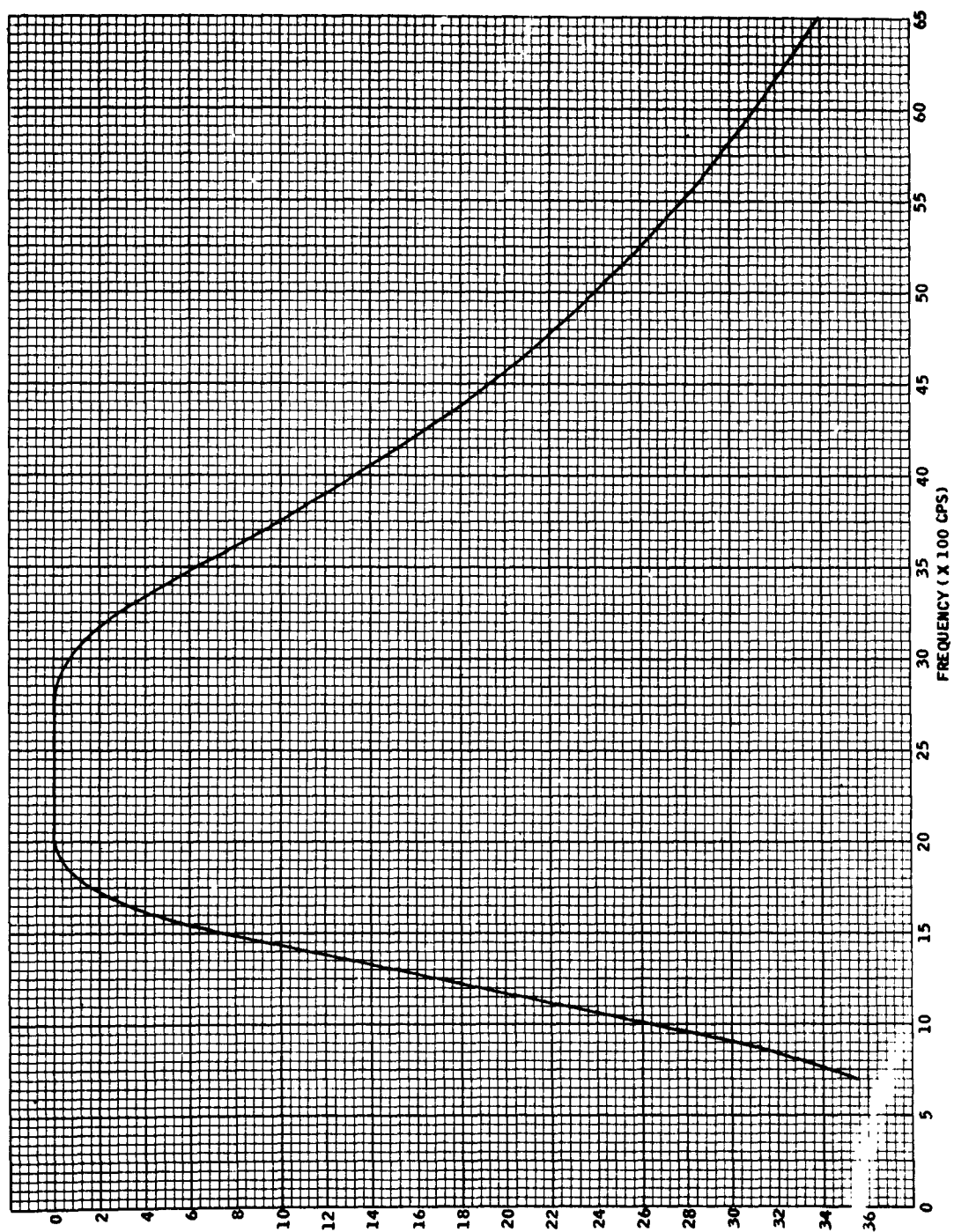
Figure 4-3. Filter Test Setup

Figure 4-4. Modulator Band Pass Filter Amplitude
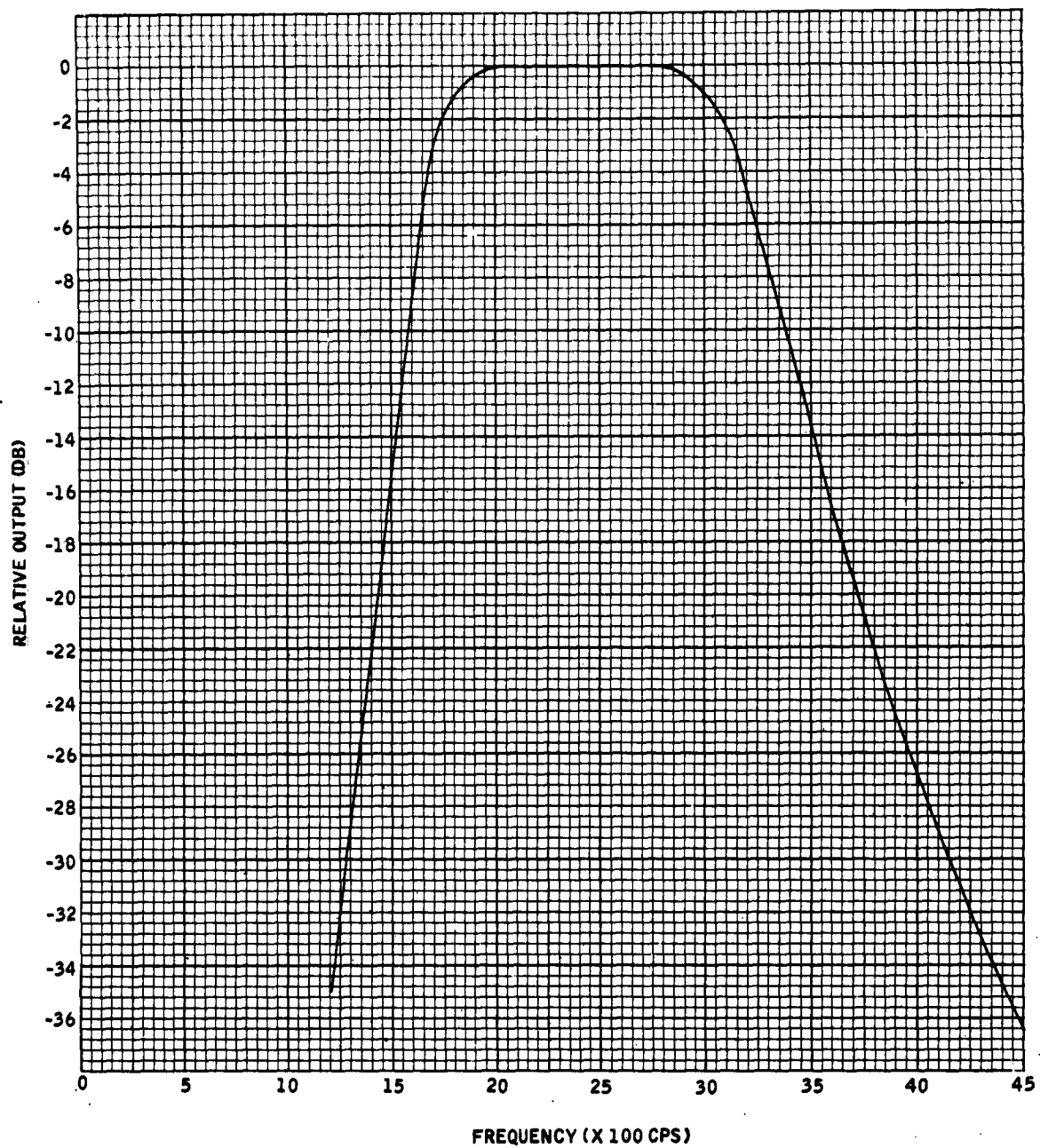Response Characteristic Curve

Figure 4-5. Demodulator Band Pass Filter Amplitude
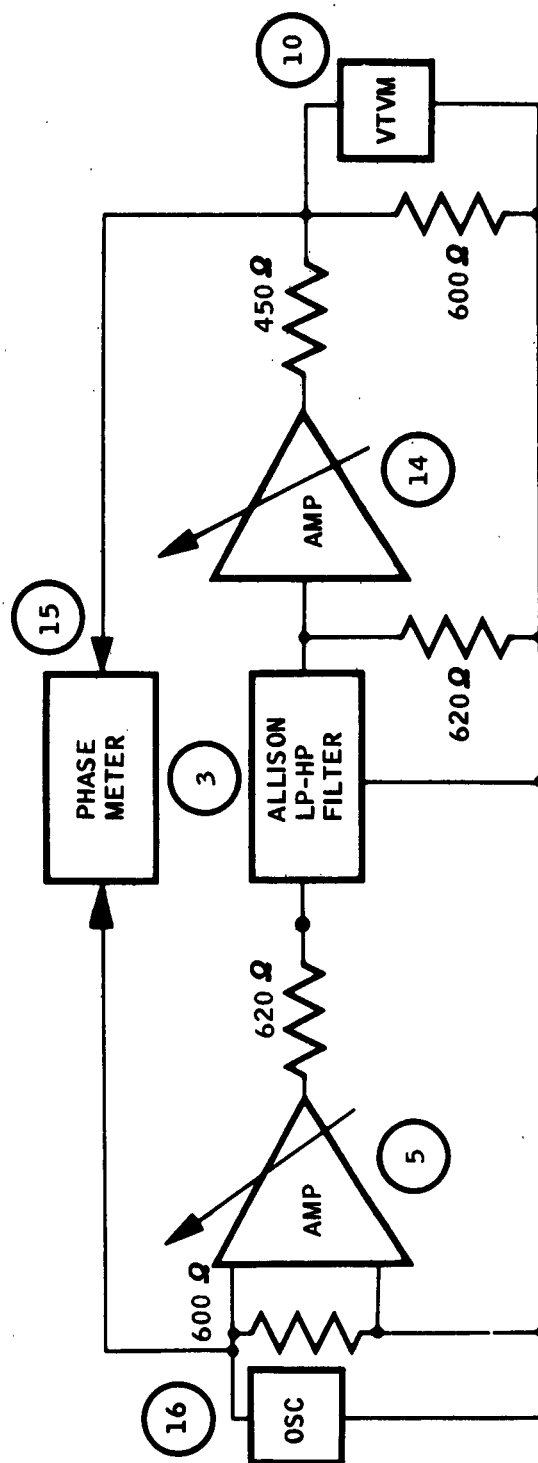Response Characteristic Curve

Figure 4-6. Test Setup for Phase Characteristic of
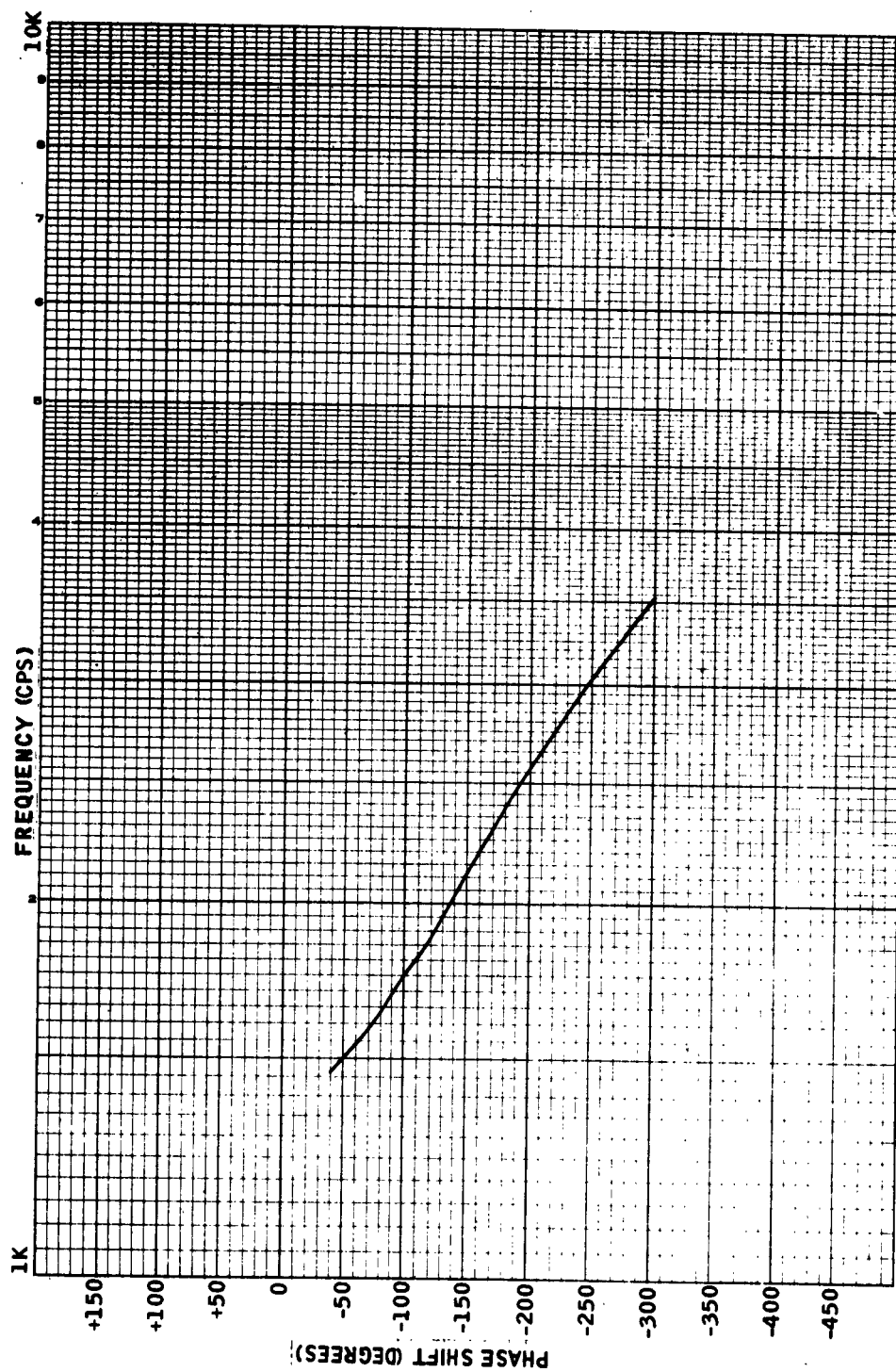Simulated 600 Ohm Transmission Line

Figure 4-7. Phase Characteristic Curve of
              Simulated 600 Ohm Transmission Line
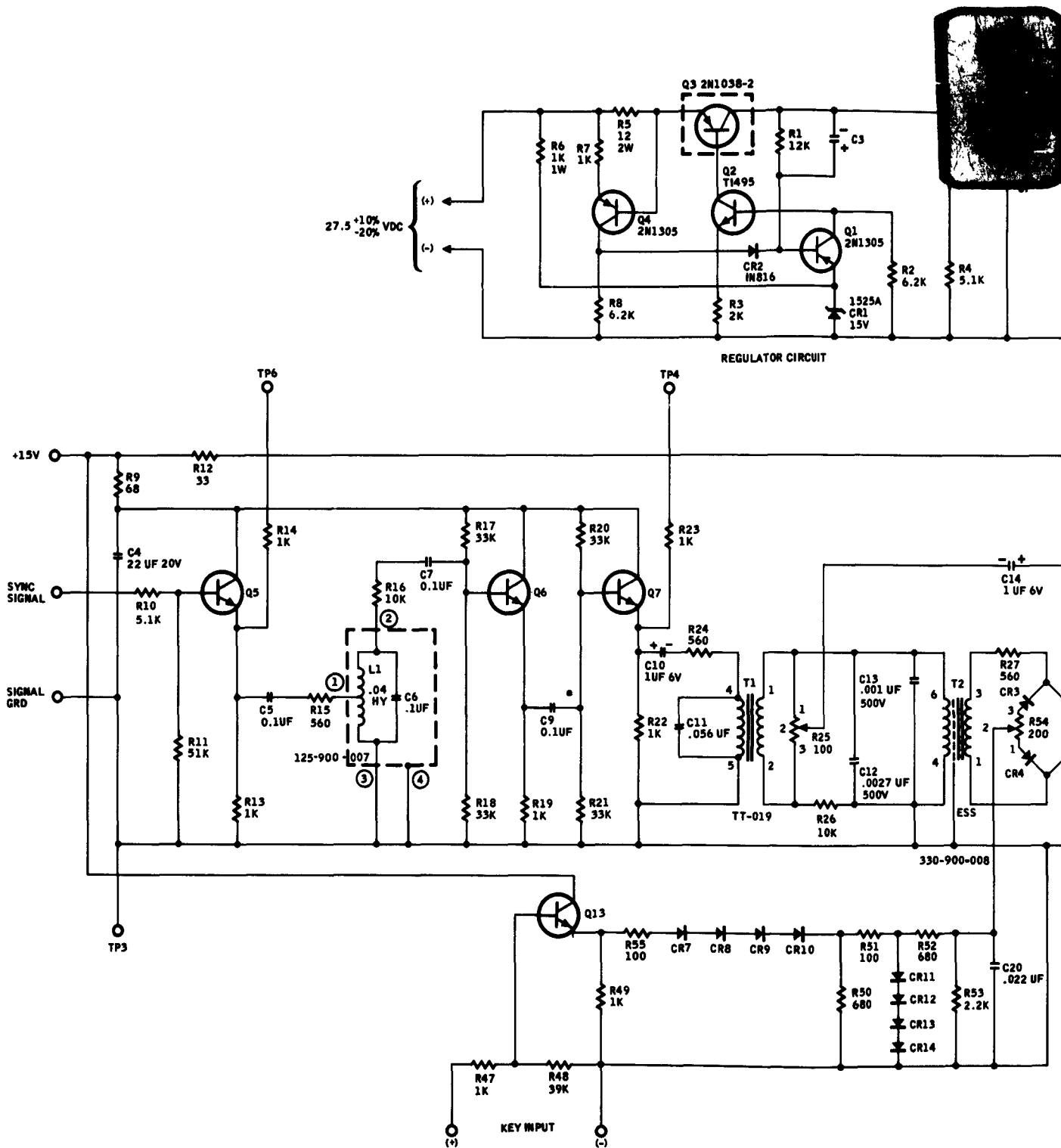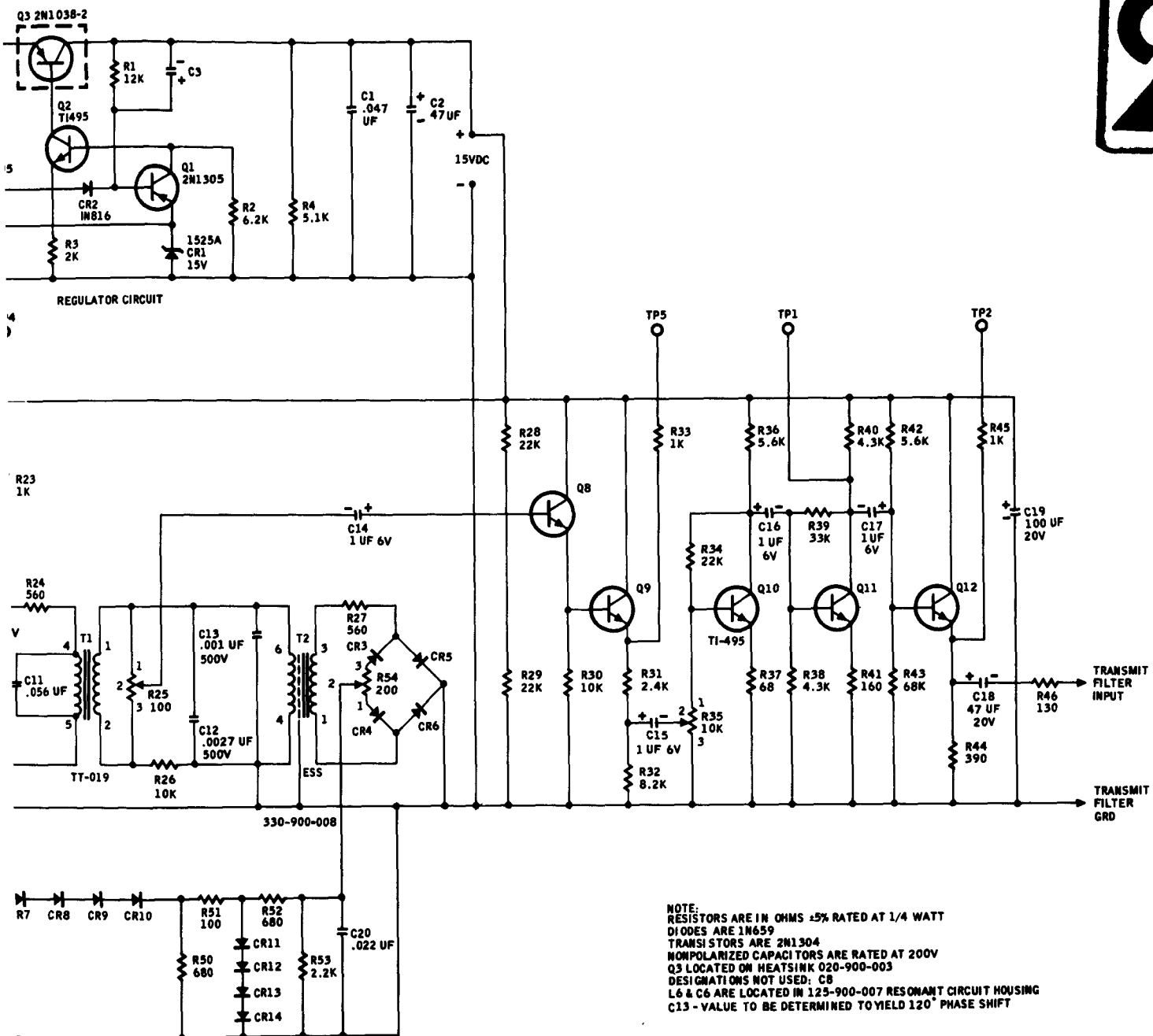
SECTION V

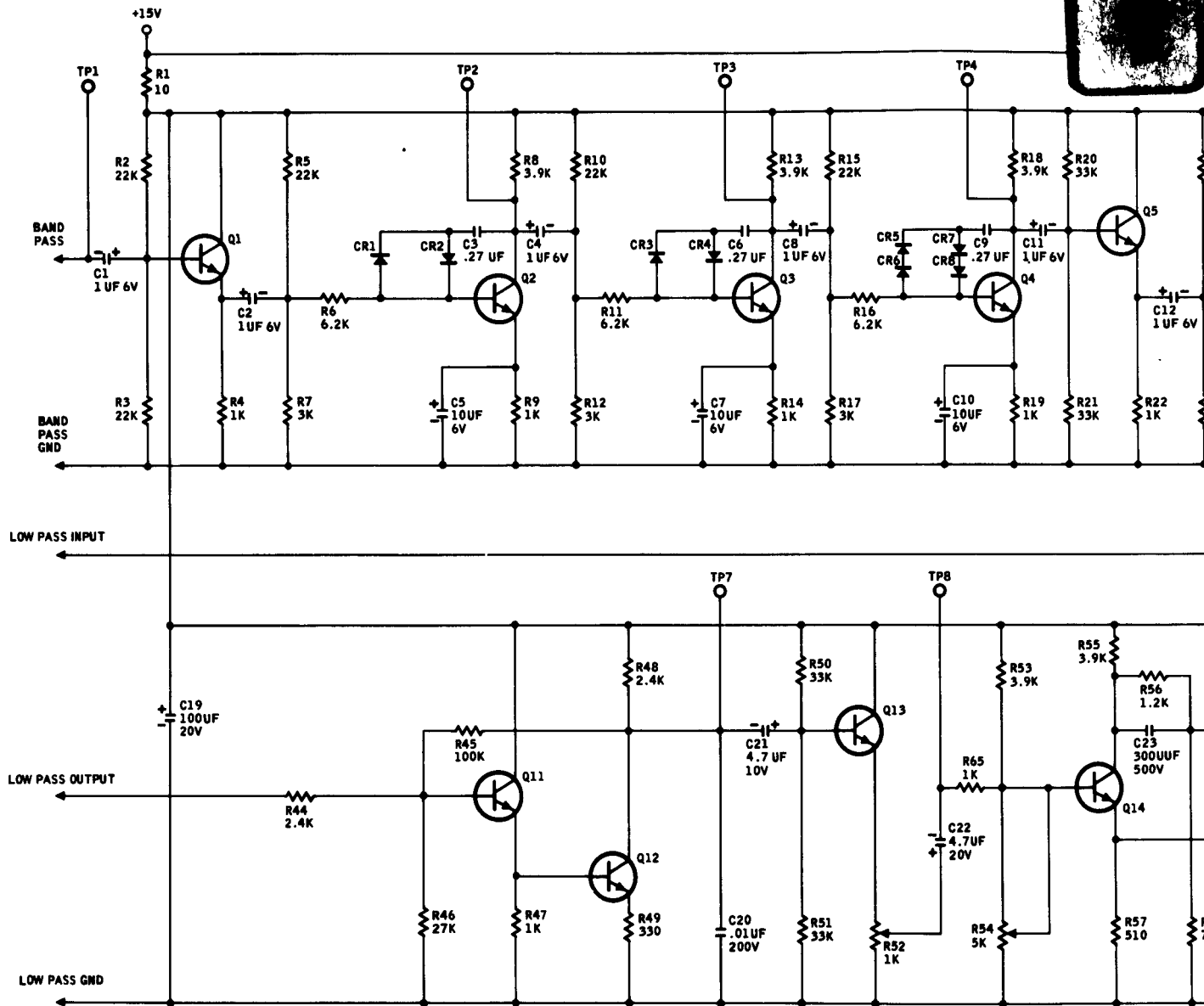DIAGRAMS

Figure 5-1. Modulator & Regulator Schematic Diagram

Q3 2N1038-2

R1 12K

C3

Q2 TI495

C1 .047 UF

C2 47 UF

15VDC

Q1 2N1305

CR2 1N816

R2 6.2K

R4 5.1K

R3 2K

1525A CR1 15V

REGULATOR CIRCUIT

TP5

TP1

TP2

R28 22K

R33 1K

R36 5.6K

R40 4.3K

R42 5.6K

R45 1K

R23 1K

C14 1 UF 6V

Q8

C19 100 UF 20V

R24 560

C13 .001 UF 500V

R27 560 CR3

CR5

R34 22K

C16 1 UF 6V

R39 33K

C17 1 UF 6V

T1

R25 3 100

T2

R54 200

Q9

Q10

Q11

Q12

C11 .056 UF

C12 .0027 UF 500V

CR4

CR6

TI-495

TRANSMIT FILTER INPUT

R29 22K

R30 10K

R31 2.4K

R37 68

R38 4.3K

R41 160

R43 68K

C18 47 UF 20V

R46 130

TT-019

R26 10K

ESS

R35 10K

C15 1 UF 6V

R44 390

330-900-008

R32 8.2K

TRANSMIT FILTER GRD

R7 CR8 CR9 CR10

R51 100

R52 680

C20 .022 UF

R50 680

CR11

CR12

R53 2.2K

CR13

CR14

NOTE:
RESISTORS ARE IN OHMS ±5% RATED AT 1/4 WATT
DIODES ARE 1N659
TRANSISTORS ARE 2N1304
NONPOLARIZED CAPACITORS ARE RATED AT 200V
Q3 LOCATED ON HEATSINK 020-900-003
DESIGNATIONS NOT USED: C8
L6 & C6 ARE LOCATED IN 125-900-007 RESONANT CIRCUIT HOUSING
C13 - VALUE TO BE DETERMINED TO YIELD 120° PHASE SHIFT

Figure 5-2. Demodulator Schematic Diagram

2

TP4 TP5

R13 3.9K R15 22K R18 3.9K R20 33K R23 22K R25 2.4K R28 1.2K R31 68K R33 820 CR9 R37 75

Q5 Q8 C14 .27UF

C8 1UF 6V CR5 CR7 C9 C11 R26 R29 C13 R35 R39 R40 Q10 C18
CR6 CR8 .27UF 1UF 6V 1.2K 1.2K 100UUF 5.6K 39K 2.2K 47
Q3 500V Q9 20V

Q4 Q6 Q7 R38 R42 R43
R16 C12 R36 1K 2.2K 100
6.2K 1UF 6V C15 5.6K
.27UF

CR10

R14 R17 C10 R19 R21 R22 R24 R27 R30 R32 R34 R41 C16 C17
1K 3K 10UF 1K 33K 1K 10K 470 750 33K 820 100 .27UF 10UF 6V
6V

TP6

TP8 TP9

R50 33K R53 3.9K R55 3.9K R60 3.9K CR12 CR14 CR16 R61 100

Q13 R56 Q15 CR13 CR15 CR17 R62 100

R65 1.2K CR18
1K C23 6.8V IW
300UUF Q14 IN 3016B
C22 500V Q16
4.7UF
20V

OUTPUT 0→6V

R51 R52 R54 R57 R58 R63 R64
33K 1K 5K 510 750 10K 1K

NOTE:
ALL DIODES ARE IN659
ALL TRANSISTORS ARE 2N1304
ALL RESISTORS ARE 1/4 W ± 5%
R59 NOT USED
CR11 NOT USED
ALL NON-POLARIZED CAPACITORS 200V

3-5/6

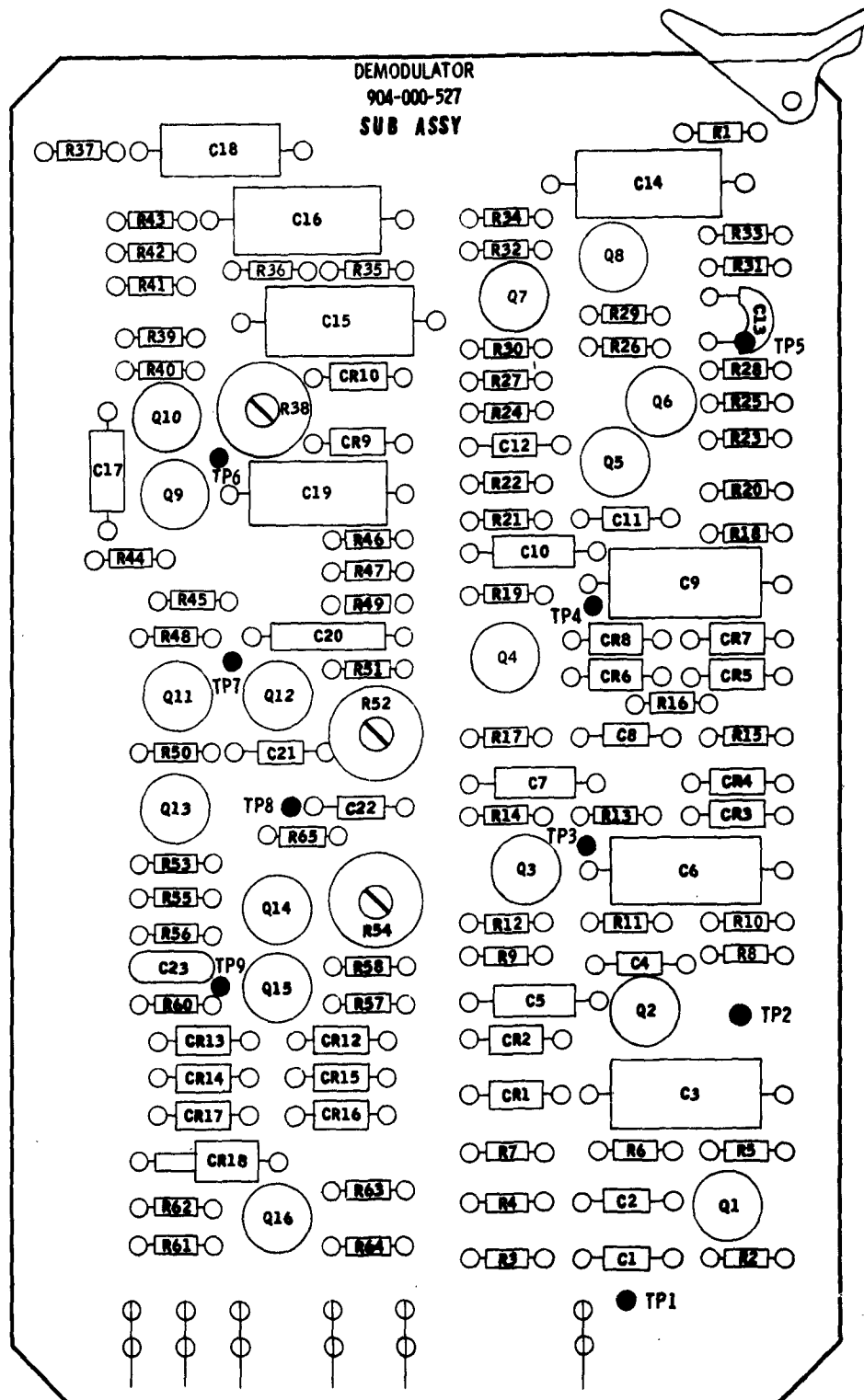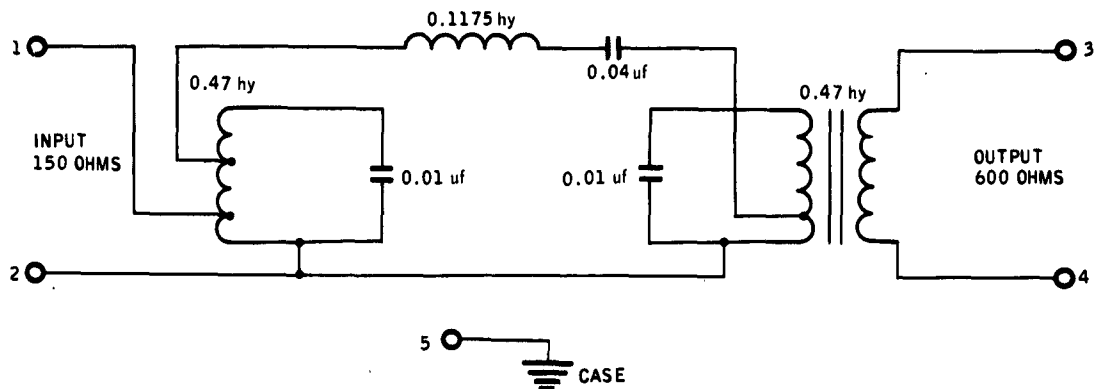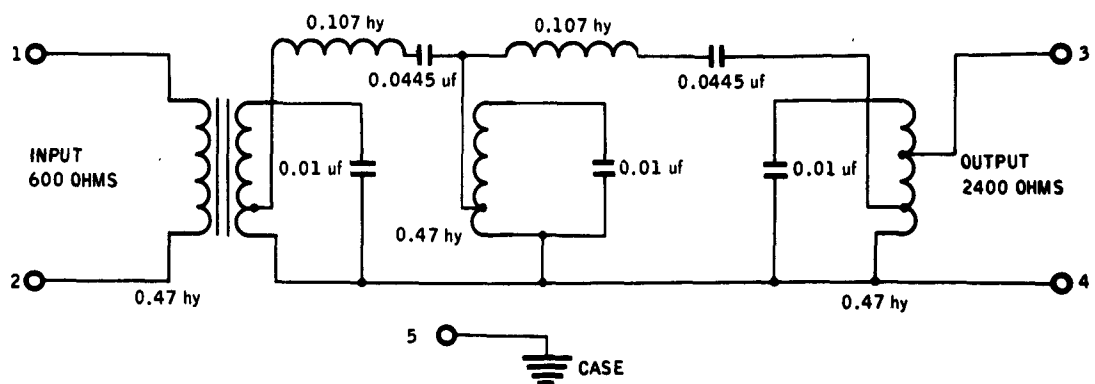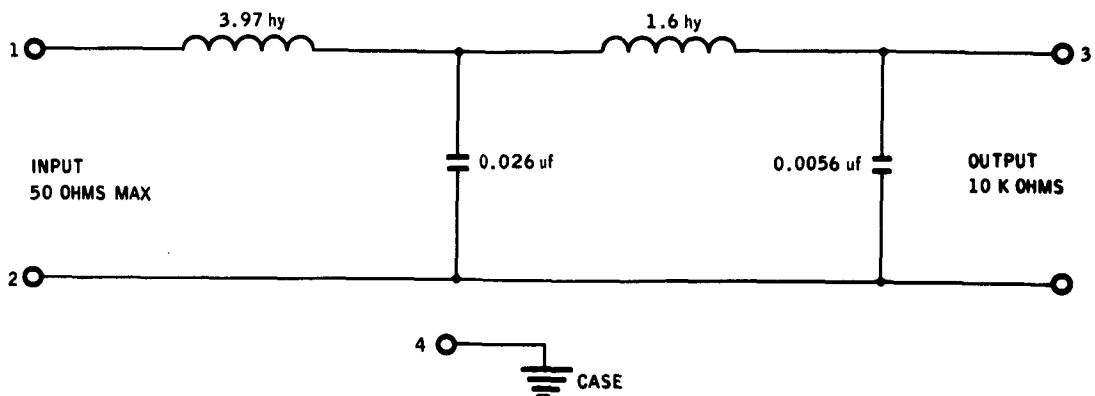Figure 5-3. Modulator and Regulator Component Layout

Figure 5-4. Demodulator Component Layout

A. MODULATOR BAND PASS FILTER PART NO. 125-900-006

B. DEMODULATOR BAND PASS FILTER PART NO. 125-900-005

C LOW PASS FILTER PART NO. 125-900-004

Figure 5-5.   Schematic Diagrams of Filters